

# Compal Confidential

## K42 / V720 / 720S DIS M/B Schematics Document

Intel KabyLake U Processor with DDR4  
N16S-GTR-S(940) (23x23mm)

2016-11-03

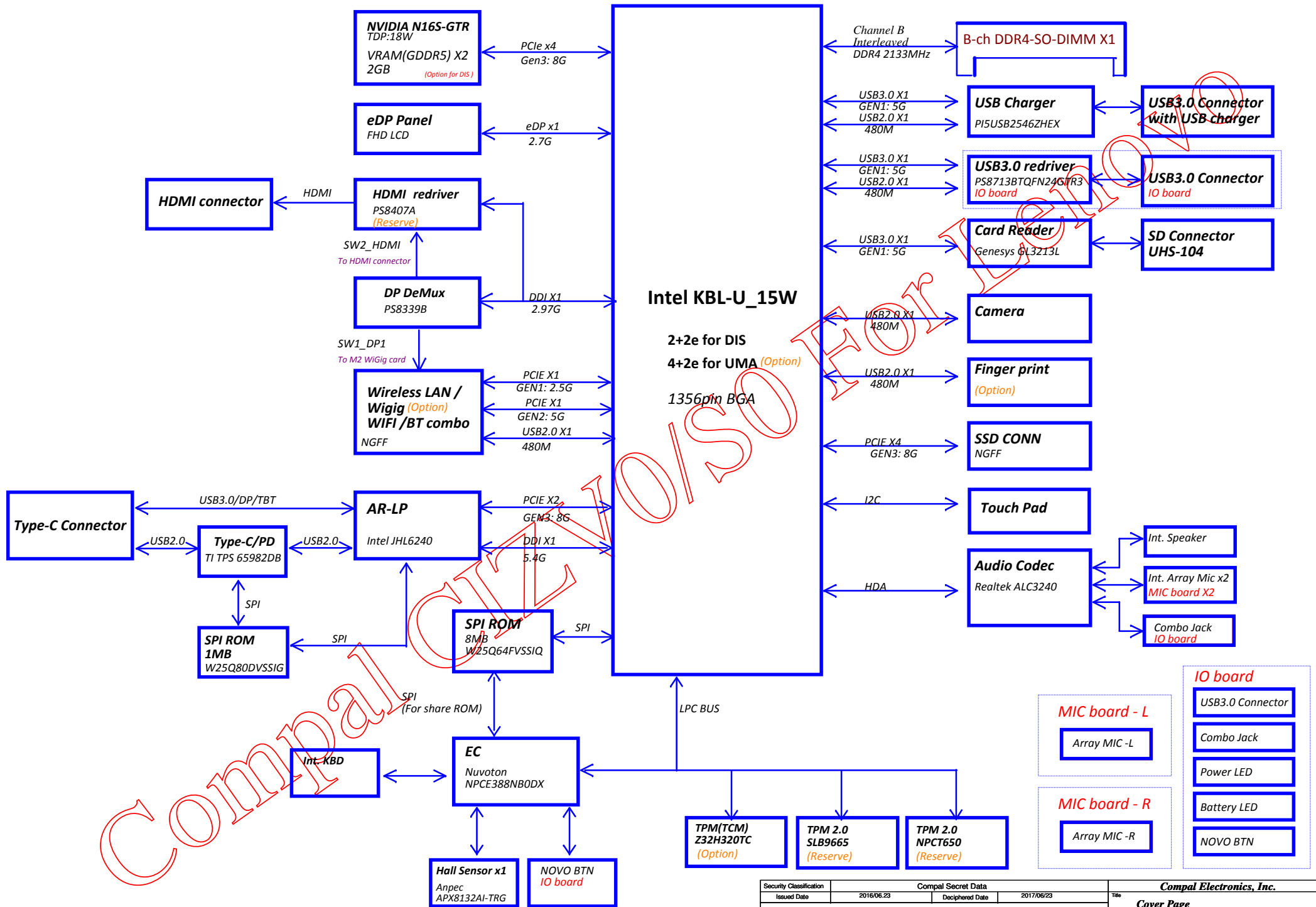
LA-E581P

REV : 0.3

ZZZ CIZV0 CIZS0 PCB PCB@

Part Number	Description
DA80019X000	PCB 1YB LA-E581P REV0 M/B 3

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## Voltage Rails

power plane	B+	+5VALW +3VALW +1.8VALW +1.0VALW	+1.2V +2.5V	+5VS +3VS +1.0VS_VCCOPC +VCCORE +VCCGT +1.0V_VCCST +1.0VS_VCCIO +1.8VS +0.6VS
State				
S0	○	○	○	○
S3	○	○	○	×
S5 S4/AC	○	○	×	×
S5 S4/ Battery only	○	×	×	×
S5 S4/AC & Battery don't exist	×	×	×	×

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Function	K42/V720-14 /720S-14 (New)
Port 1	WiGig
Port 2	WLAN
Port 3	Thunderbolt
Port 4	Thunderbolt
Port 5	NGFF_SSD_Lane3
Port 6	NGFF_SSD_Lane2
Port 7	NGFF_SSD_Lane1
Port 8	NGFF_SSD_Lane0
Port 9	DGPU_Lane 1
Port 10	DGPU_Lane 2
Port 11	DGPU_Lane 3
Port 12	DGPU_Lane 4
Port 13	N/A
Port 1A	N/A
Port 1B	N/A
Port 2	N/A

Function	K42/V720-14 /720S-14 (New)
Port 1	USB2_External_Port (Type-C)
Port 2	USB2_External_Port (USB3)
Port 3	USB2_External_Port (IO BD)
Port 4	N/A
Port 5	Camera
Port 6	Finger Print
Port 7	NGFF_BT
Port 8	N/A
Port 9	N/A
Port 10	N/A
Port 1	Type-C_External_Port
Port 2	USB3_External_Port
Port 3	USB3_External_Port
Port 4	CardReader
Port 5	N/A
Port 6	N/A

## SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	SODIMM	Thermal Sensor	Touch Pad	Touch Screen	PCH	TypeC-PD
EC_SMB_CLK1 EC_SMB_DA1	NPCE388 +3V1	X	V	V	X	X	X	X	X	V
EC_SMB_CLK2 EC_SMB_DA2	NPCE388 +3VS	V	X	X	X	Reserve	X	X	V	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VS	X	X	X	V	X	X	X	X	X
I2C1_SCL_TS I2C1_SDA_TS	PCH +3VS	X	X	X	X	X	X	Reserve	X	X
I2C0_SCL_TP I2C0_SDA_TP	PCH +3VS	X	X	X	X	X	V	X	X	X
Address	Write Read	0X9E			0XA4 0XA3	0X4C	0X2C			0X38

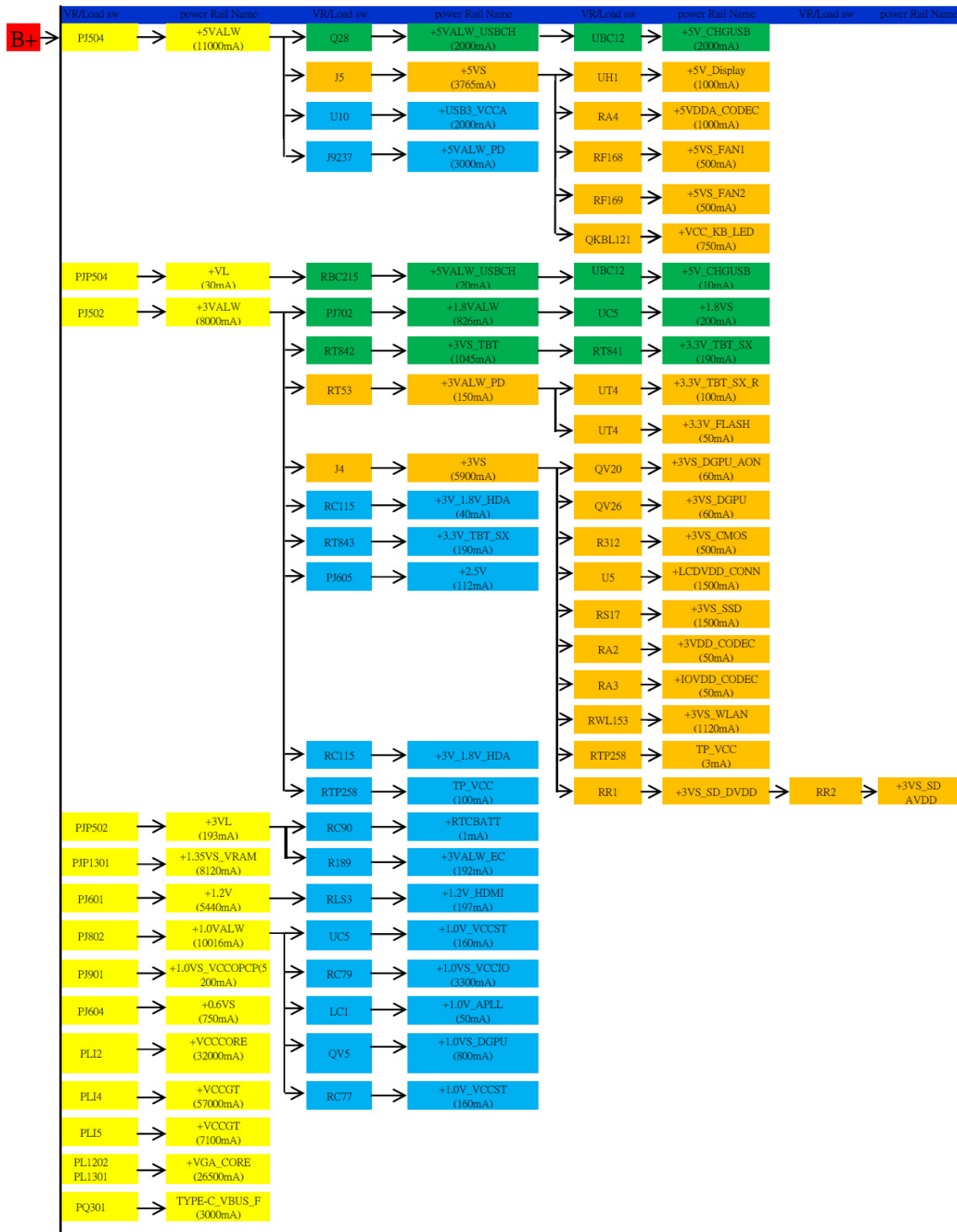
## BOM Structure Table

Item	BOM Structure
For PCB part number	PCB@
For 2+2e CPU	22E@
For 4+2e CPU	42E@
For EMI mount on 2+2e CPU	22E_EMI@
For EMI mount on 4+2e CPU	42E_EMI@
For DIS SKU	DIS@
For UMA SKU	UMA@
For NV GC6	GC6@
For NV NoGC6 (Reserve)	NOGC6@
For CIZV0 MB 1D	CIZV0@
For CIZS0 MB 1D	CIZS0@
For W/ DP/HDMI MUX SKU	MUX@
For W/O DP/HDMI MUX SKU	NOMUX@
For W/ HDMI re-dirver	LS@
For W/O HDMI re-dirver	NOLS@
For W/ W/O HDMI re-dirver	NOMUXNoLS@
For W/7 camera support	CMOS@
For W/10 camera support	NOCMOS@
For W/ KB Back Light	KBL@
For W/O KB Back Light	NOKBL@
For Thunderbolt	TBT@
For Fingrt Print SKU	FP@
For ESD mount on Fingrt Print SKU	FP_ESD@
For Intel WiGig Card SKU	WiGig@
For Nationz TCM SKU	TCM@
For EMI mount on TCM/TPM SKU	TCM_EMI@
For Infineon/Nuvoton TPM (Reserve)	TPM@/TPM@
For No TCM/TPM SKU	NOTPM@
For CIZV0 NO TPM X4E	V0_NOTPM@
For CIZS0 NO TPM X4E	S0_NOTPM@
For Thermal Sensor (Reserve)	THM@
For Intel DCI Debug	DCI@
For Debug Card	DeBug@
For HDMI Logo	45@
For ESD mount on CIZV0 HDMI SKU	HDMI_ESD@
For EMI mount component	EMI@
For EMI un-mount component	@EMI@
For ESD mount component	ESD@
For ESD un-mount component	@ESD@
For RF mount component	RF@
For RF un-mount component	@RF@
For ME Connector	ME@
For VRAM X76 BOM	X76@
For Hynix 2G VRAM	H2G@
For Hynix 2G VRAM (R1 P/N)	H2G_R1@
For Hynix 2G VRAM (R3 P/N)	H2G_R3@
For Micron 2G VRAM	M2G@
For Micron 2G VRAM (R1 P/N)	M2G_R1@
For Micron 2G VRAM (R3 P/N)	M2G_R3@
For Samsung 2G VRAM	S2G@
For Samsung 2G VRAM (R1 P/N)	S2G_R1@
For Samsung 2G VRAM (R3 P/N)	S2G_R3@

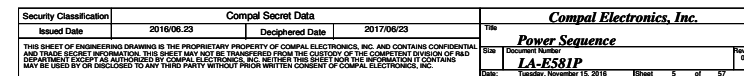
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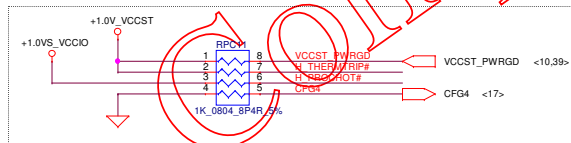
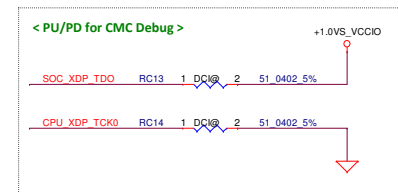
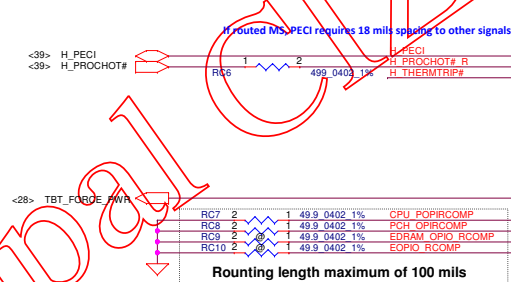
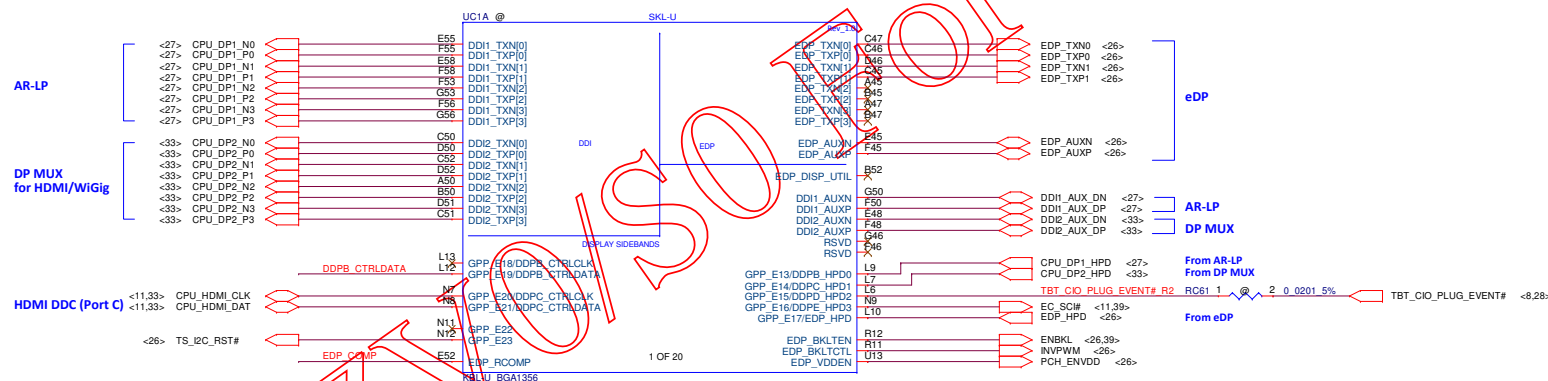
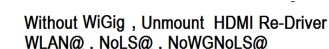
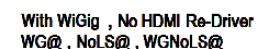
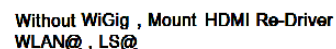
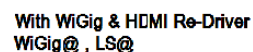


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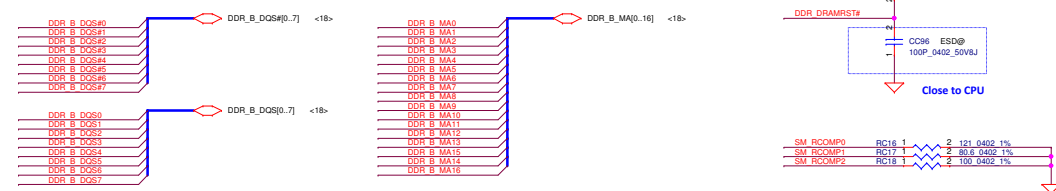
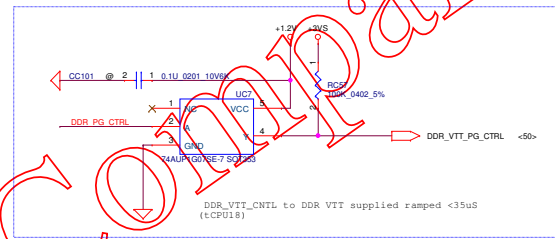
For Lenovo





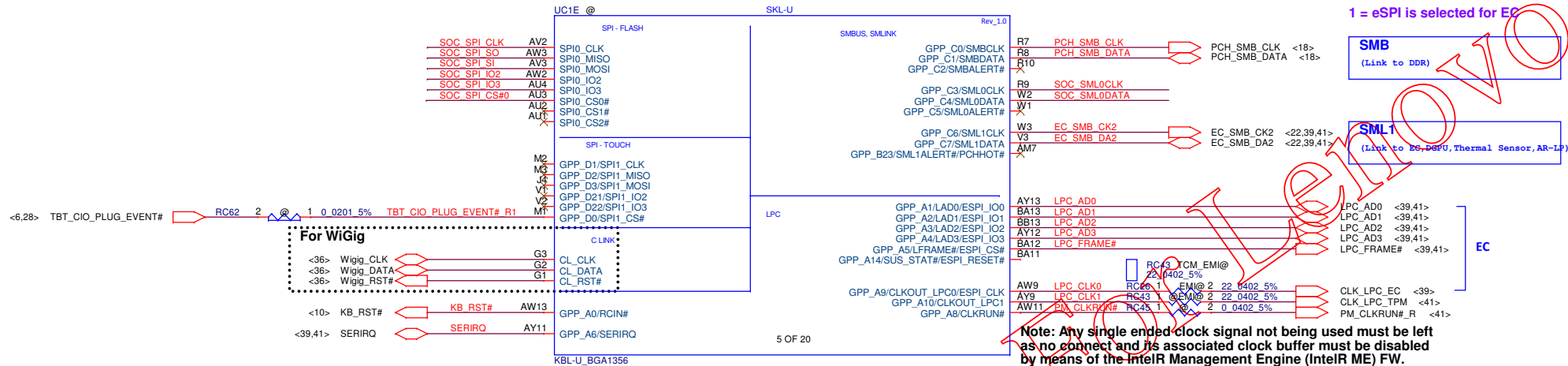
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# Interleaved Memory



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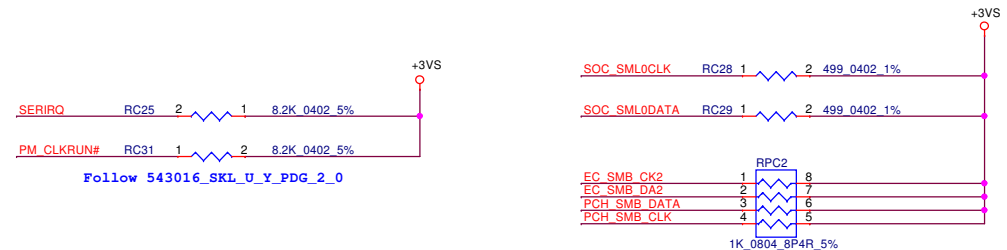
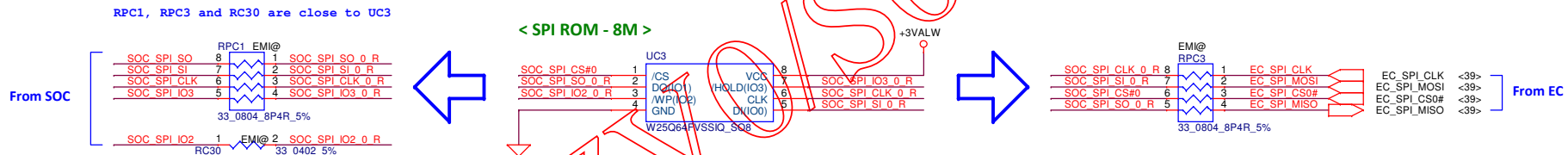


SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

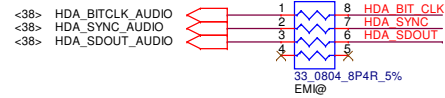
1 = eSPI is selected for EC



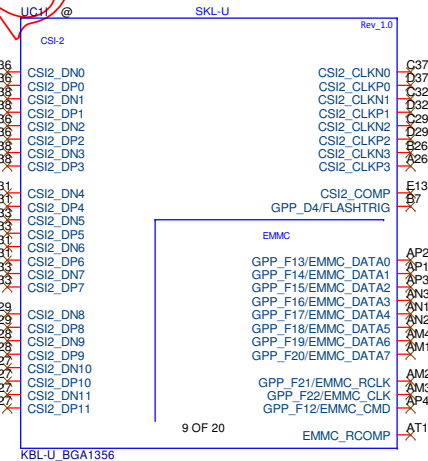
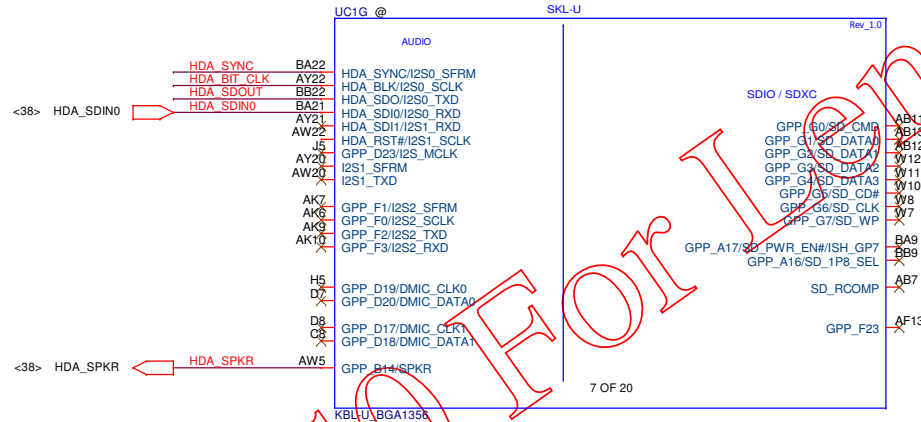
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< HD AUDIO >

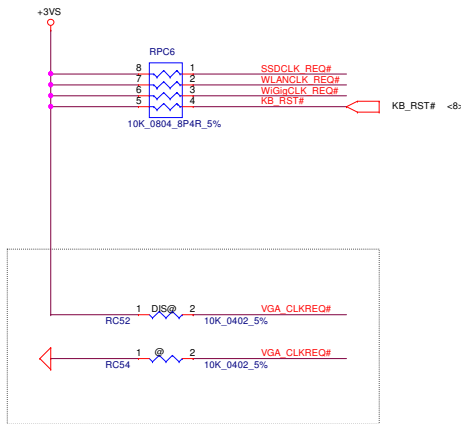


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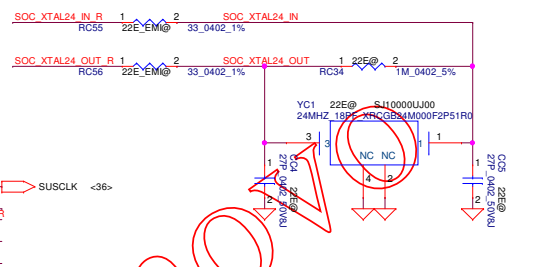
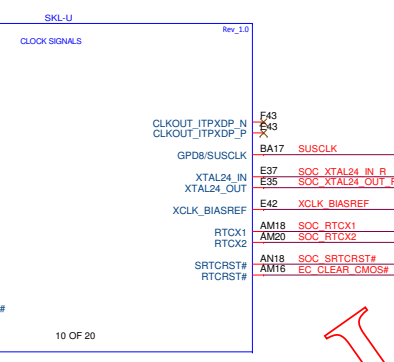
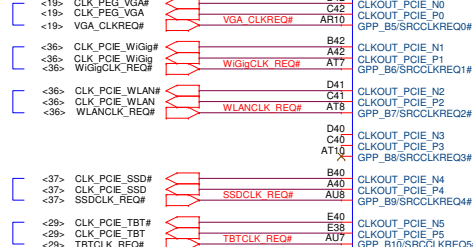


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Note: Any differential clock pair not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel® Management Engine (Intel® ME) FW.

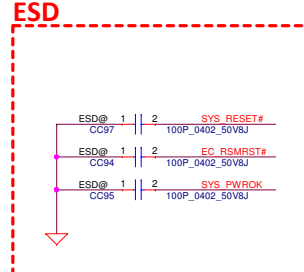
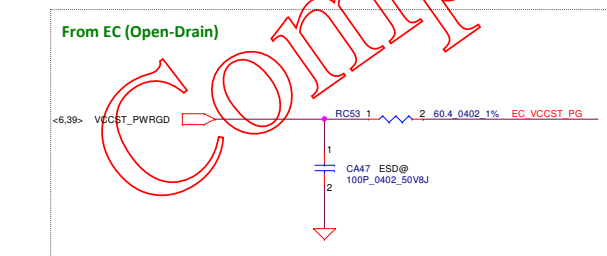
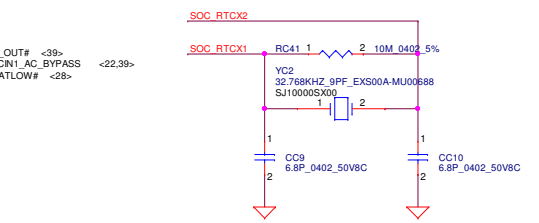
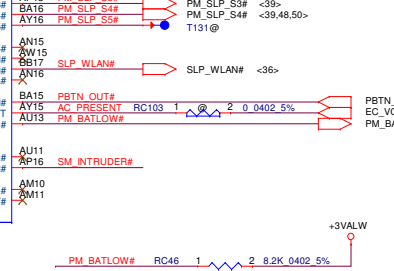
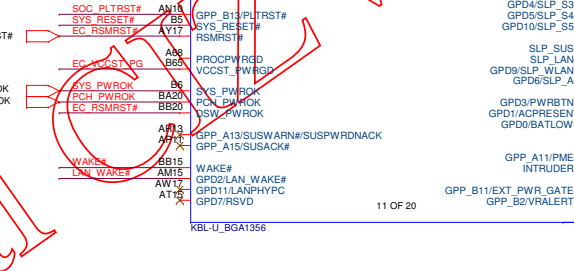
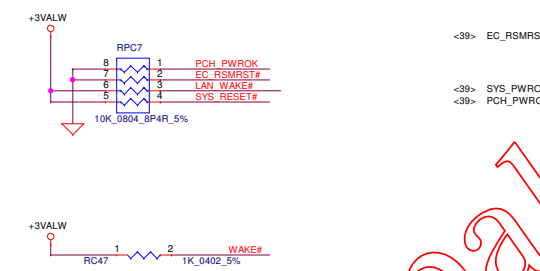
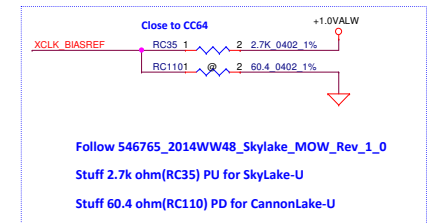
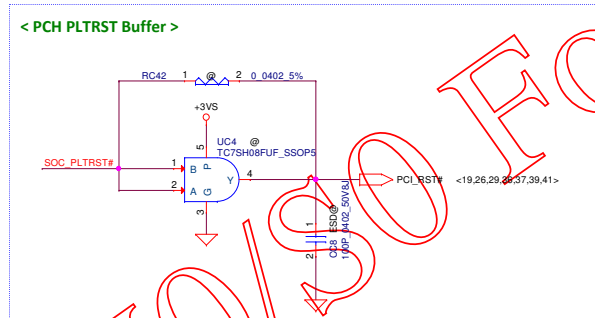
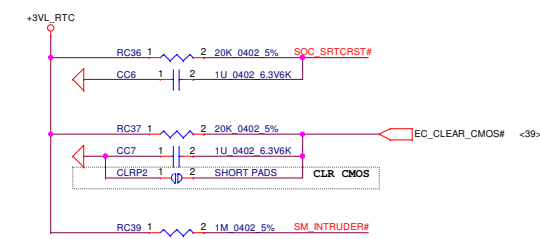


DGPU  
WiGig (KEY E)  
NGFF BT (KEY A)  
SSD  
AR-LP



Parameter	Symbol	Recommended Value	Max./Min. Range	Condition
Frequency	f <sub>0</sub>	24MHz		@25°C
Vibration Mode		Fundamental		
CUT		AT		
Loading		Parallel resonant		
Frequency Tolerance @25°C	Df/f <sub>0</sub> @25°C	±35ppm		@25°C ±3°C
Temperature Stability	Df/f <sub>0</sub>	±30ppm		10° to 70°C
Aging	Df/f <sub>0</sub>	±5ppm		
Crystal Loading	C <sub>load</sub>	18-20pF		
Shunt capacitance	C <sub>s</sub>			6pF Max
Drive Level	D <sub>L</sub>		200uW Min	
Series Resistance	R <sub>s</sub>		50Ω or less	@25°C

Note:  
1. Customers should verify that the vendor's published specifications in the component data sheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective data sheet.  
2. Perform performance testing and EMC (FCC and EN) testing in real systems.  
3. Independently measure the component's electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.



## GPIO\_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode, ==> Default

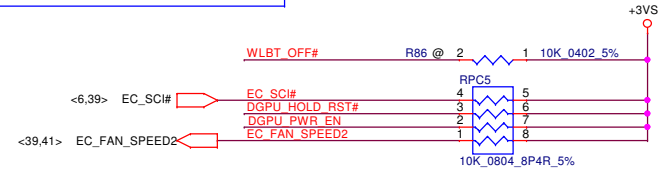
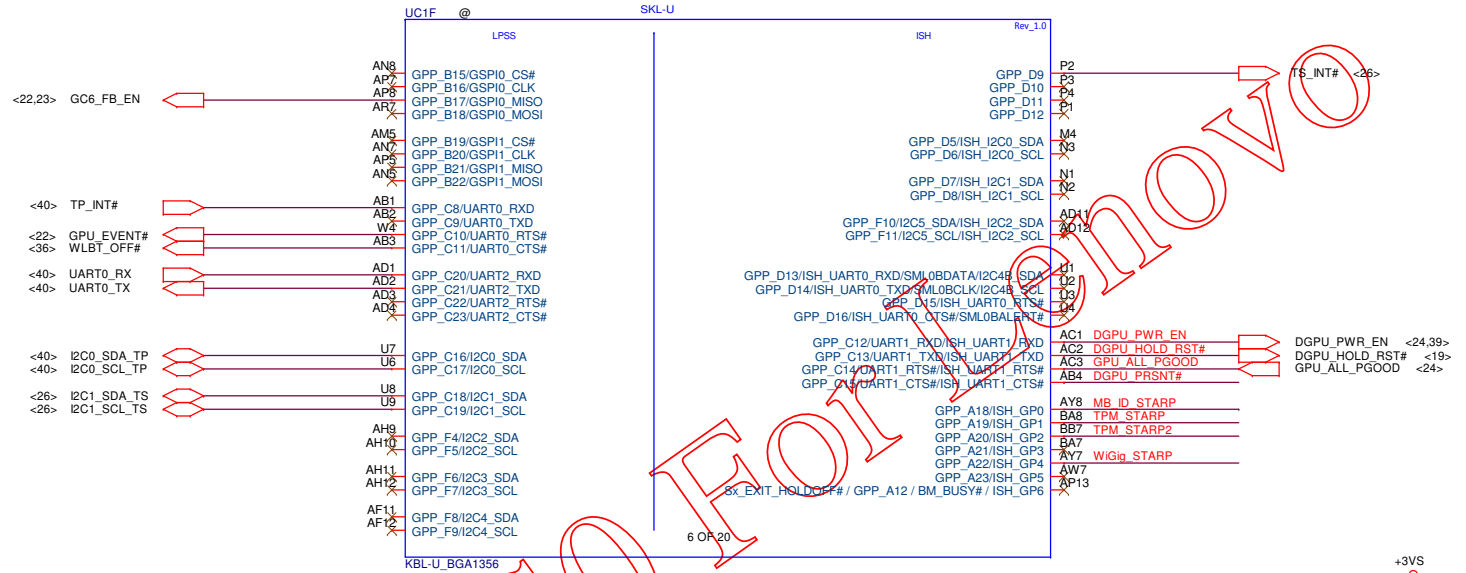
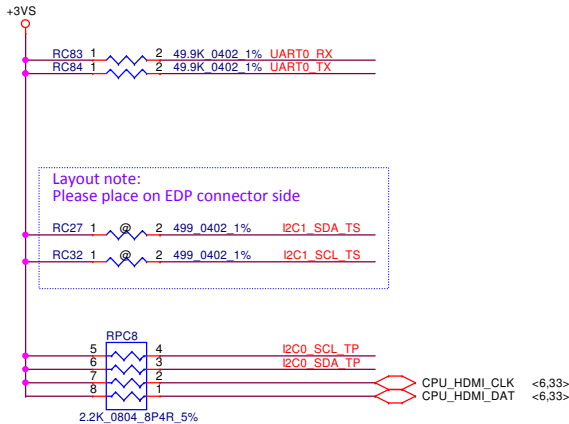
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

## GPIO\_MOSI (Internal Pull Down):

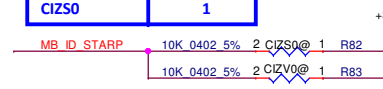
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

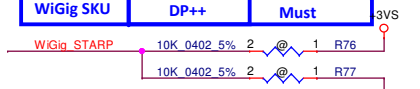
1 = LPC Mode



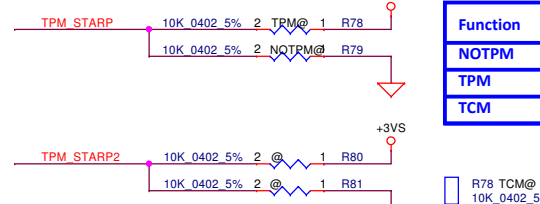
Function	MB_ID (GPP_A18)
CIZV0	0
CIZS0	1



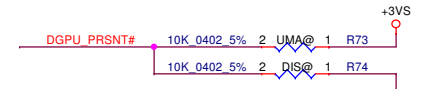
Function	DDI2 Interface	PCH_GPPA22
WLAN SKU	HDMI	WiGig_STARP
WiGig SKU	DP++	Reserve



Function	PCH [GPPA20,GPPA19]
NOTPM	[X, 0]
TPM	[X, 1]
TCM	[X, 1]



Function	DGPU_PRSTNT# (GPP_C15)
DIS	0
UMA Only	1



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WiGig  
(NGFF)

WLAN  
(NGFF)

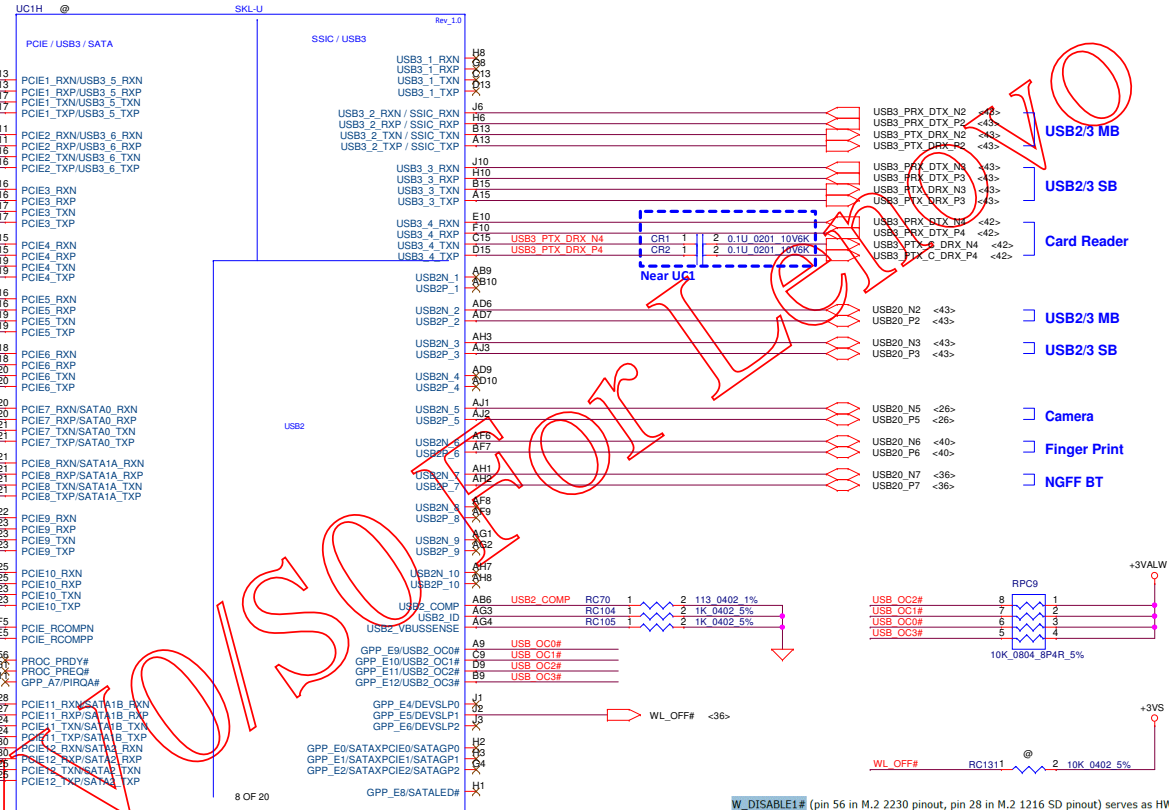
AR-LP

SSD

dGPU

Function	K42/V720-14 /720S-14 (New)
PCIe2.0/3.0	Port 1 WiGig
	Port 2 WLAN
	Port 3 Thunderbolt
	Port 4 Thunderbolt
	Port 5 NGFF_SSD_Lane3
	Port 6 NGFF_SSD_Lane2
	Port 7 NGFF_SSD_Lane1
	Port 8 NGFF_SSD_Lane0
	Port 9 DGPU_Lane 1
	Port 10 DGPU_Lane 2
	Port 11 DGPU_Lane 3
	Port 12 DGPU_Lane 4
SATA	Port 0 N/A
	Port 1A N/A
	Port 1B N/A
	Port 2 N/A

Function	K42/V720-14 /720S-14 (New)
USB 2.0	Port 1 USB2_External_Port (Type-C)
	Port 2 USB2_External_Port (USB3)
	Port 3 USB2_External_Port (IO BD)
	Port 4 N/A
	Port 5 Camera
	Port 6 Finger Print
	Port 7 NGFF_BT
	Port 8 N/A
	Port 9 N/A
	Port 10 N/A
USB 3.0	Port 1 Type-C_External_Port
	Port 2 USB3_External_Port
	Port 3 USB3_External_Port
	Port 4 CardReader
	Port 5 N/A
	Port 6 N/A



When PCIe8/SATA1A is used as SATA Port 1 (QDD), then PCIe11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

W\_DISABLE1# (pin 56 in M.2 2230 pinout, pin 28 in M.2 1216 SD pinout) serves as HW RF kill for the Bluetooth radio.

Table 2-2 W\_DISABLE1# characteristics

Characteristic	Description
Internal pull up resistor	min 100 kOhm, max 200kOhm
VIL for Asserting	min 0V, max 0.6V
VIH for De-asserting	min 1.26V, max 3.3V or float (not connected)

### 2.2.2.1 M.2 Bluetooth HW RF kill

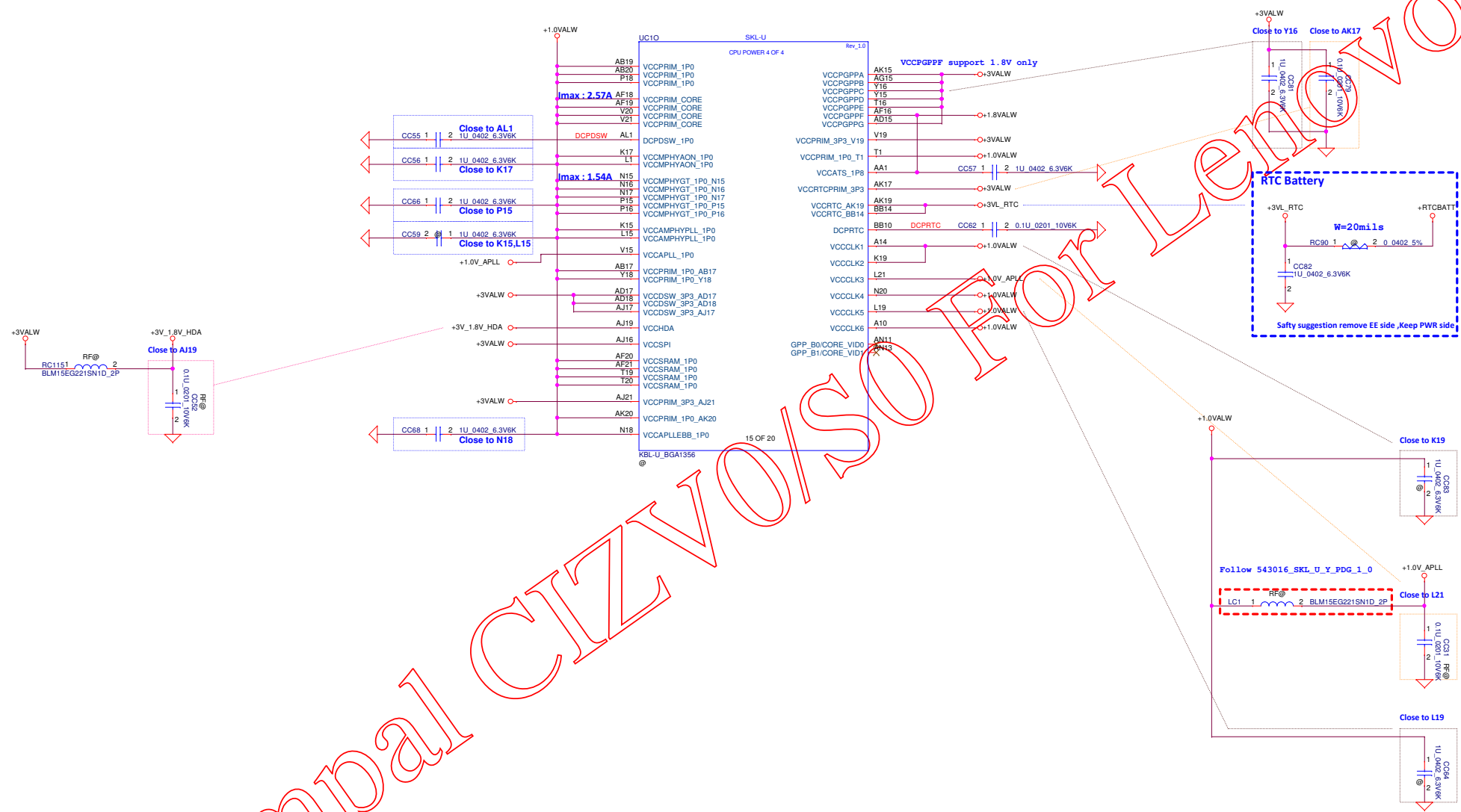
W\_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216 SD pinout) serves as HW RF kill for the Bluetooth radio.

Asserting W\_DISABLE#\_2 signal will result in a complete shutdown of the Bluetooth part. The result from the user perspective is similar to removing the Bluetooth device from the laptop.

Table 2-3 W\_DISABLE2# characteristics

Characteristic	Description
Internal pull up resistor	min 100 kOhm, max 200kOhm
VIL for Asserting	min 0V, max 0.6V
VIH for De-asserting	min 1.26V, max 3.3V or float (not connected)



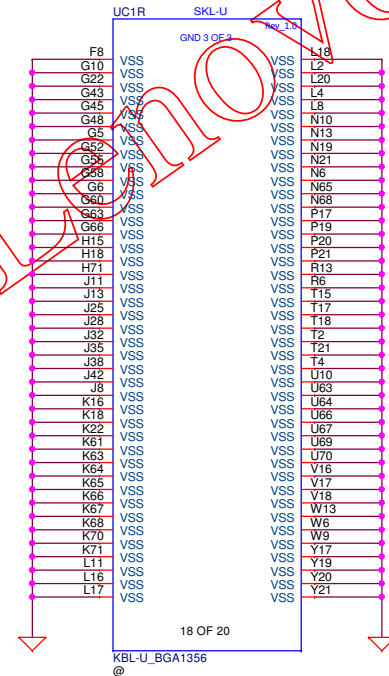
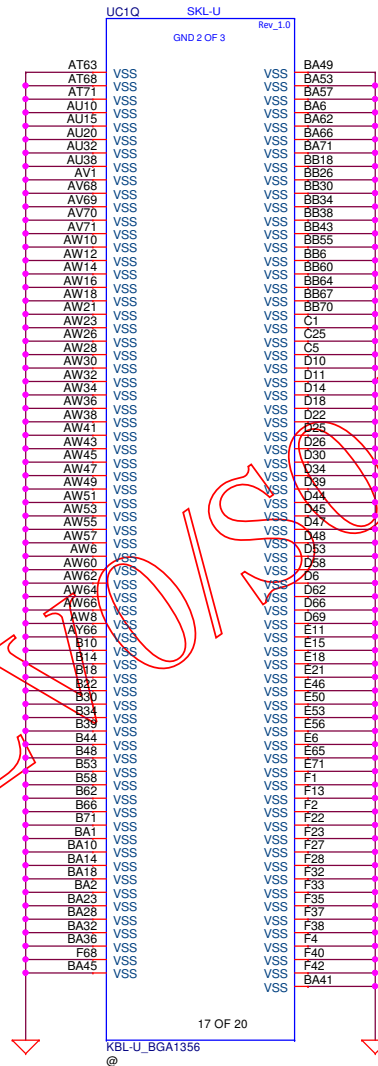
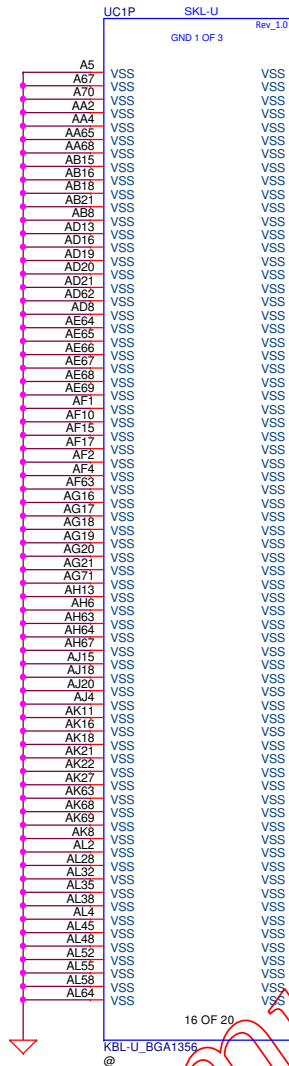


Security Classification		Compal Secret Data		Title	
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2016/06/23		2017/06/23		Document Number	
				LA-E581P	
				Rev	
				0.1	
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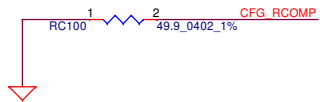




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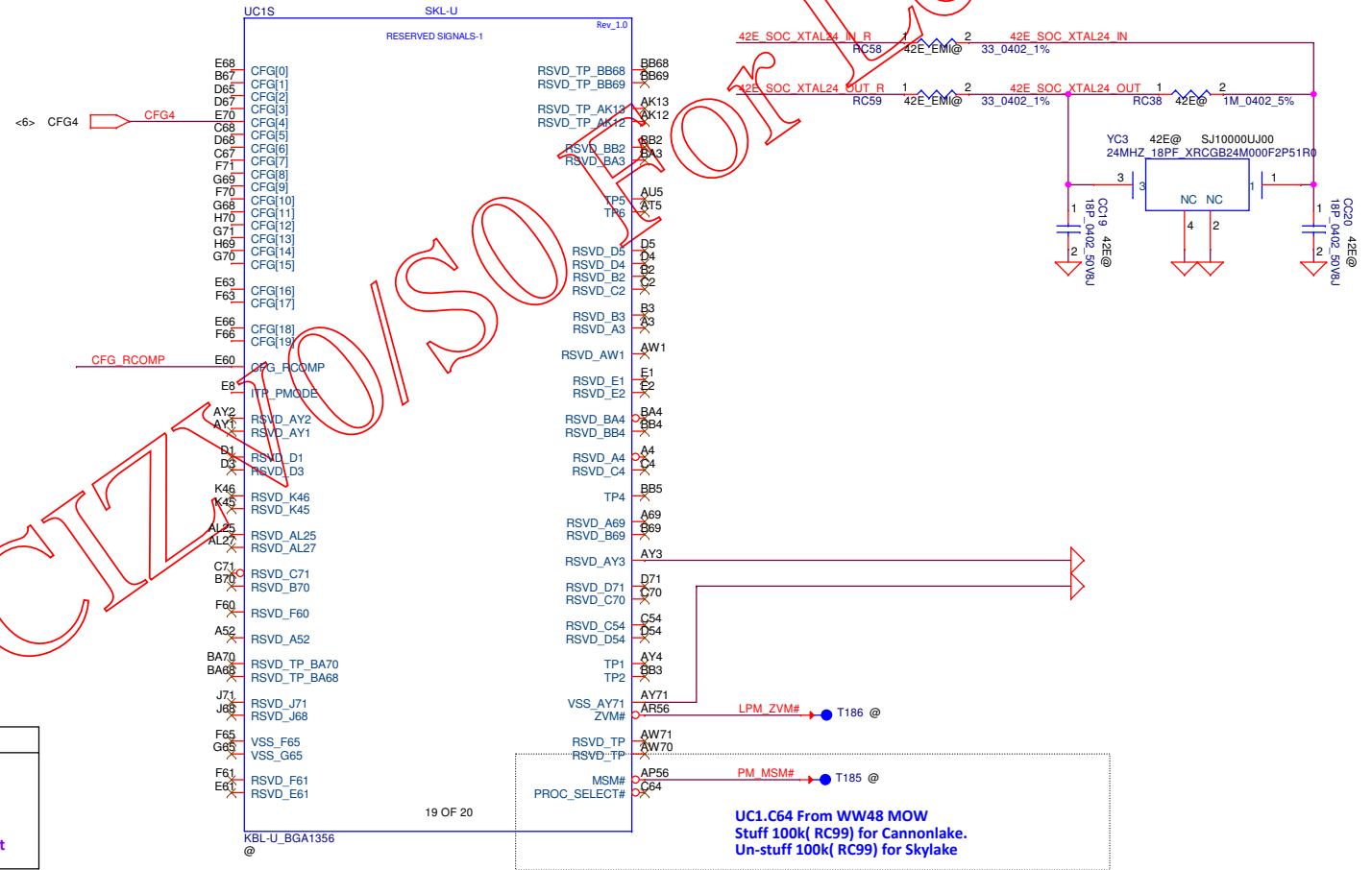
# Processor/PCH Strapping Checklist (Sheet 1 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted.	Connect a series 1 K resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.
CFG[1]	Reserved. No connect.	
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal. A test point may be placed on the board for it.	1 = Normal operation. 0 = Lane numbers reserved.
CFG[3]	Reserved configuration lane.	
CFG[4]	Display Port Presence strap.	1: Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0: Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.
CFG[6:5]	PCI Express* Bifurcation. A test point may be placed on the board for it.	00 = 1x8, 2x4 PCI Express* 01 = reserved. 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*
CFG[7]	PEG Training. A test point may be placed on the board for them.	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.



## Display Port Presence Strap

CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
------	---

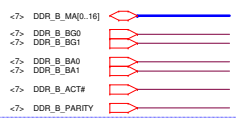


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				Size
				Document Number
				LA-E581P
				Rev
				0.1
				Date: Tuesday, November 15, 2016
				Sheet 17 of 57

## CLK



## CMD



## Alert



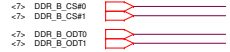
## SMBUS



## Strobe



## CTRL



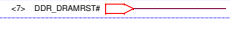
## CKE



## Data

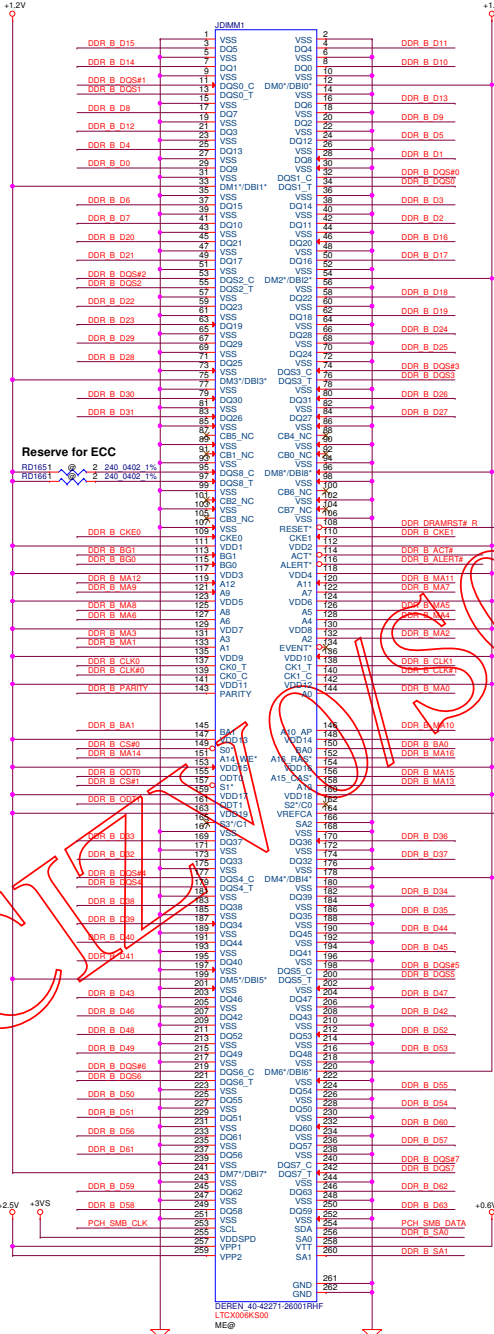
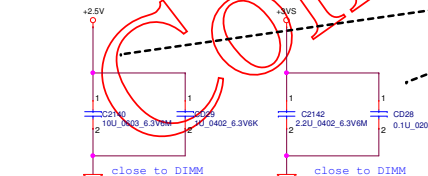
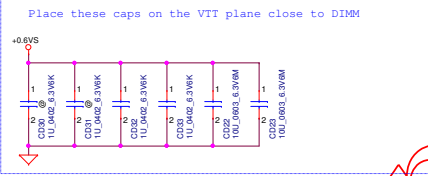
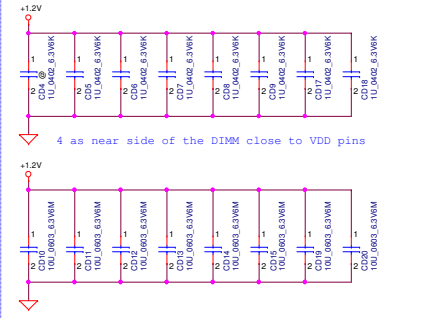


## Reset



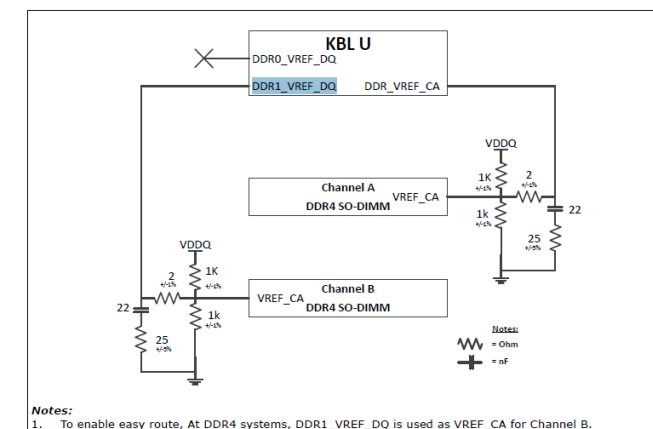
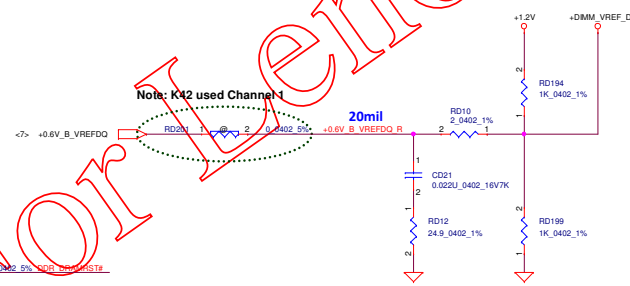
Layout Note:  
Place near JDIMM1

Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



## Reverse Type

2-3A to 1 DIMMs/channel



Notes:  
1. To enable easy route, At DDR4 systems, DDR1\_VREF\_DQ is used as VREF\_CA for Channel B.

SPD ADDRESS FOR CHANNEL B :

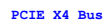
WRITE ADDRESS: 0XA4

READ ADDRESS: 0XA3

SA0 = 0; SA1 = 1; SA2 = 0.

DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S

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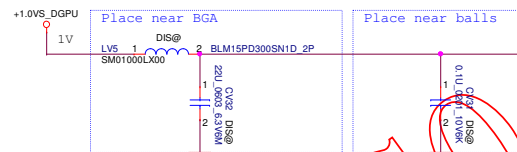
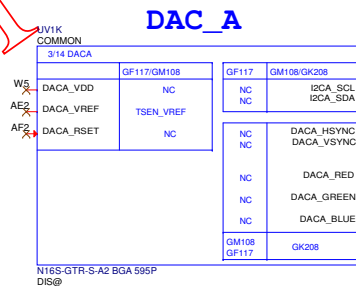
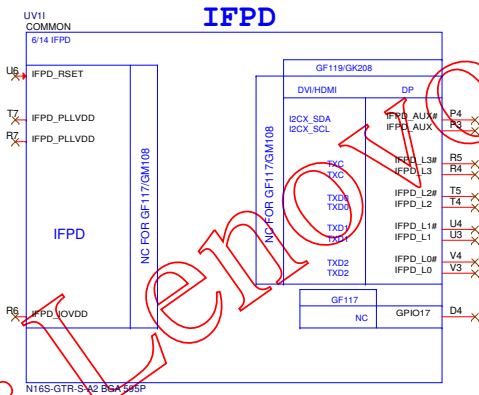
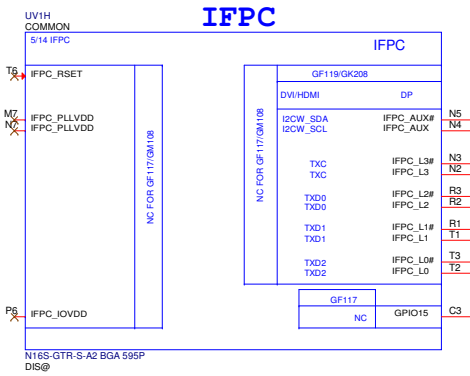
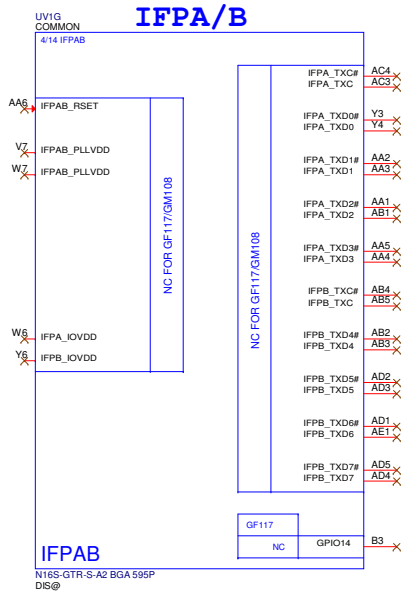
GPU Package Type	Capacitor Type	Footprint	Population	Location
GR2B-64/ GR2-64	1.0 $\mu$ F X6S	0402	1	Under GPU
	4.7 $\mu$ F X6S	0603	1	Near GPU
	10 $\mu$ F X5R	0805	1	Midway between GPU and Power Supply
	22 $\mu$ F X5R	0805	1	Midway between GPU and Power Supply

Table 3-18. PEX\_SVDD\_3V3 and PEX\_PLL\_HVDD Decoupling

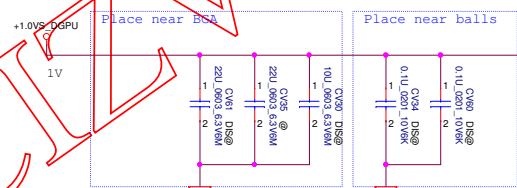
Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X7R	0402	1	Near GPU
4.7 $\mu$ F	X5R	0603	2	Near GPU

Table 3-17. PEX\_PLLVDD Decoupling

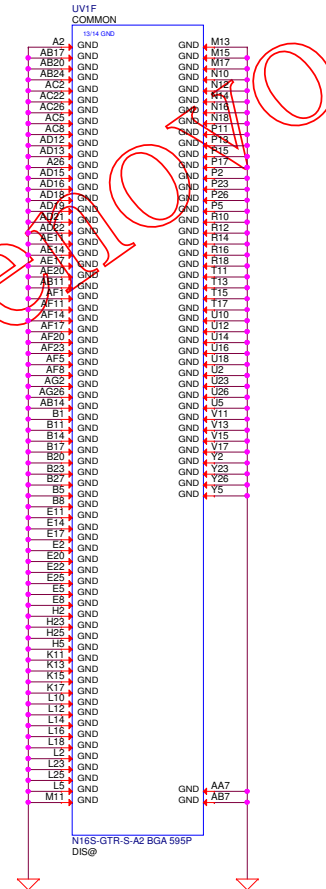
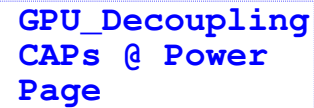
Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X7R	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU



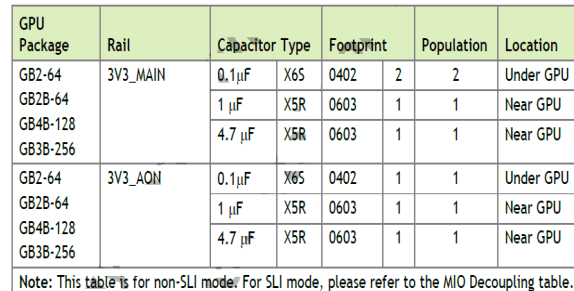
GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128	PLLVD	0.1 μF X7R	0402	1	Under GPU
		22 μF X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.05 Ω)	0402	1	Near GPU







N16S-GTR-S-A2 BGA 595P  
DIS@



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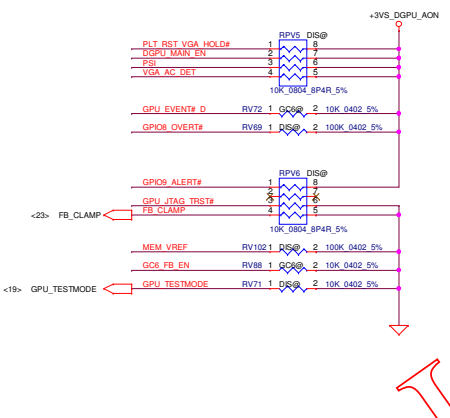
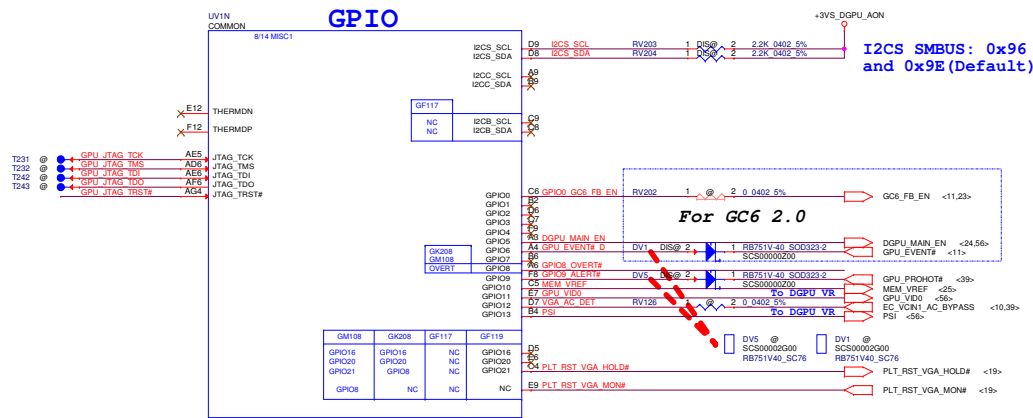
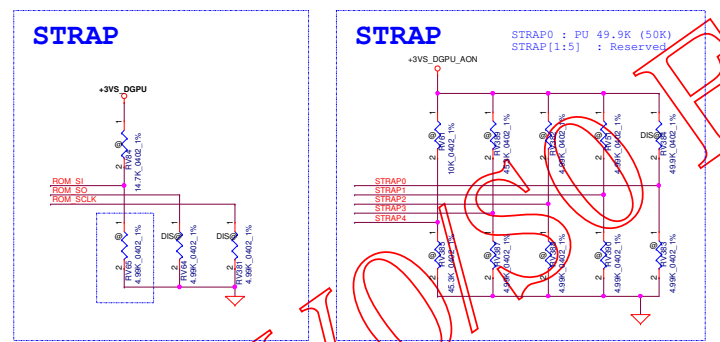
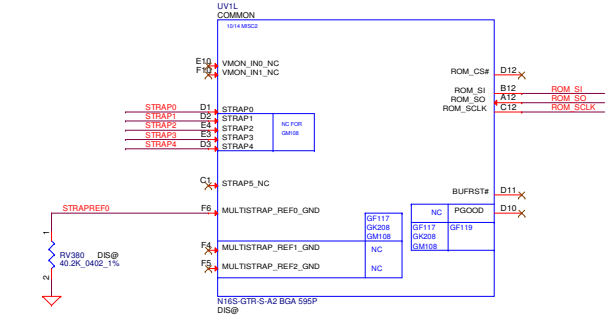


Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	MQ Termination
GPIO0	GCA_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDDQ float voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3D_Vision	O	3D Vision I/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System self-reset monitor	10 kΩ pull-up to 3V3_AON unless actively driven
GPIO9	THERM_ALERT	I/O	Active thermal alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VDD	O	GPU core VDD PWM control signal	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	MC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase
GPIO14	HPD_A	I	Hot Plug Detect for IFA used as DisplayPort for IFAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFBF or IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



Item	N16P-GT	N16S-GT-B/S
Device ID	0X139A	0x1347
Package	GB4B-128	GB4B-128/GB2B-64
Internal P/N	GM107-750,28nm	GM108-755/655,28nm
ROM_SI	Refer to N16x_RAM_Straps table	Refer to N16x_RAM_Straps table
ROM_SO	0x0000, 4.99Kohm pull down	0x0000, 4.99Kohm pull down
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)
Strap2	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)
Strap3	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)
Strap4	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)
Open_VRG SKU	B	B
NVVDD Boot Voltage	0.9V	0.9V

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

RAM\_CFG[3:0] (ROM\_SI)

0x0	4.99K (L)	S2G
0x1	10.0K (L)	M2G
0x2	15.0K (L)	
0x3	20.0K (L)	
0x4	24.9K (L)	
0x5	30.1K (L)	H2G
0x6	34.8K (L)	
0x7	45.3K (L)	
0x8	4.99K (H)	
0x9	10.0K (H)	
0xA	15.0K (H)	
0xB	20.0K (H)	
0xC	24.9K (H)	
0xD	30.1K (H)	
0xE	34.8K (H)	
0xF	45.3K (H)	

#### Samsung\_X76

U18	S2G_R1@ SA000094R00	256M32 K4G80325FB-HC03
U17	S2G_R1@ SA000094R00	256M32 K4G80325FB-HC03

#### Micron\_X76

U18	M2G_R1@ SA000096K00	256M32 MT51J256M32HF-60-A
U17	M2G_R1@ SA000096K00	256M32 MT51J256M32HF-60-A

#### Hynix\_X76

U18	H2G_R1@ SA000092G00	256M32 H5GCB824MUR-T2C
U17	H2G_R1@ SA000092G00	256M32 H5GCB824MUR-T2C

U18	S2G_R3@ SA000024R20	K4G80325FB-HC03_FBA170
U17	S2G_R3@ SA000024R20	K4G80325FB-HC03_FBA170

U18	M2G_R3@ SA000096K20	256M32 MT51J256M32HF-60-A
U17	M2G_R3@ SA000096K20	256M32 MT51J256M32HF-60-A

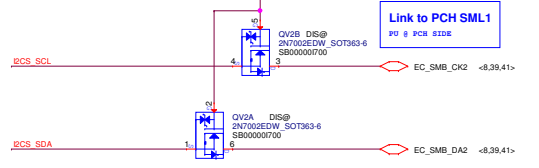
U18	H2G_R3@ SA000092G10	256M32 H5GCB824MUR-T2C
U17	H2G_R3@ SA000092G10	256M32 H5GCB824MUR-T2C

Table 12. N16V-GMR1 and N16S-LG-/GMR-/GTR GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Data Code Minimum	Status	
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready	
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready	
			Hynix	H5GC4H24JR-T2C	A-die	0x6	2500	N/A	Production ready	
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready	
			Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready	
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready	
		128Mx32	Hynix	H5GC4H24JR-T2C	A-die	0x6	2500	N/A	Production ready	
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready	
			256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
				Hynix	H5GC8H24MR-T2C	M-die	0x5	2500	N/A	Post production ready
				Micron	MT51J256M32HF-60-A	A-die	0x1	2500	N/A	Production ready
			512Mx16	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
Hynix	H5GC8H24MR-T2C	M-die		0x5	2500	N/A	Post production ready			
Micron	MT51J256M32HF-60-A	A-die		0x1	2500	N/A	Production ready			

Note: For N16V-GMR1 and N16S-LG-/GMR-/GTR, the maximum allowable memory case temperature is 85 °C.

#### Internal Thermal Sensor



#### 10.2.1 Unconnected Signals (NC)

Do not route unused FC signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 kΩ resistors.

#### 10.2.2 I<sup>2</sup>C Slave Address

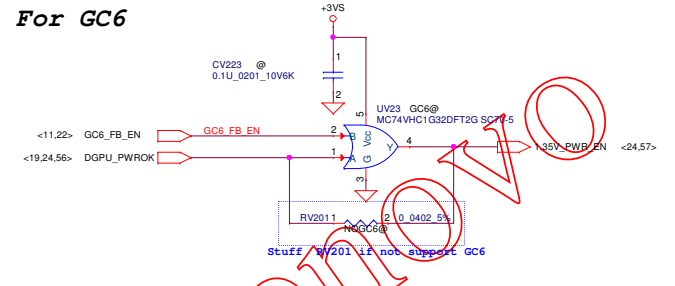
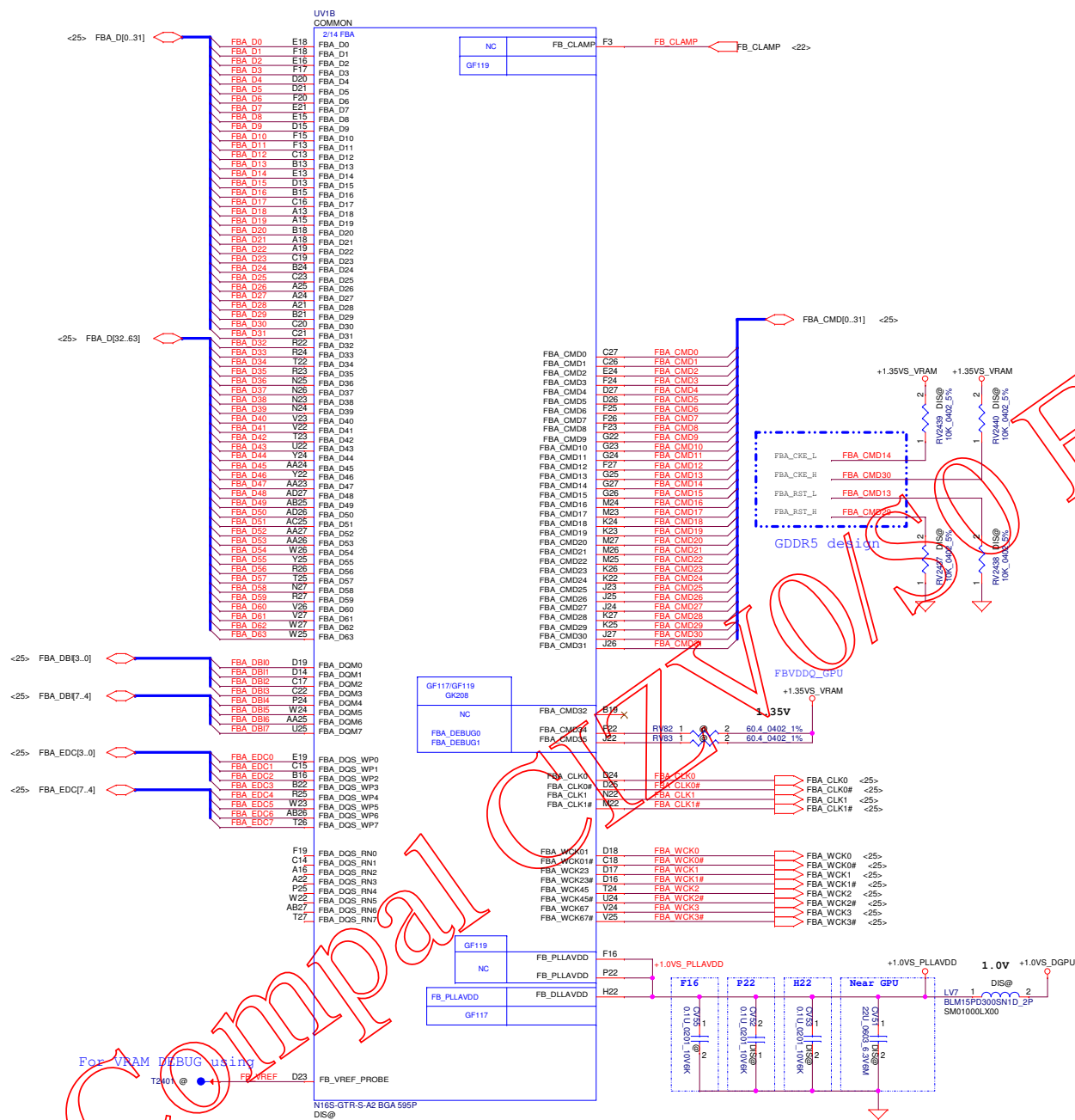
N16x GPUs use the I<sup>2</sup>C slave address 0x6h for NVIDIA internal testing. FC address 0x6h must not be used by other FC devices on the same bus as the GPU to avoid address conflict. The SMB\_ALT\_ADDR strap does not affect this 0x6h address. Refer to Chapter 15 (Straps) for a list of useful I<sup>2</sup>C Slave addresses can be used with SMB\_ALT\_ADDR strapping.

#### 16.3.3 Internal Thermal Sensor Interface

The internal thermal sensor can be accessed through the I<sup>2</sup>C interface as described in the FC chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the I<sup>2</sup>C interface by the system is not supported. The default port address to access the internal thermal sensor over the I<sup>2</sup>C is 0x9E. Table 16-1 describes the byte-wise registers accessible through the I<sup>2</sup>C interface.

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### From DG-07158-001\_v05 (NVIDIA Spec) 7.1.8 CKE\* Signal

Two copies of the clock enable signal (CKE\*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE\* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

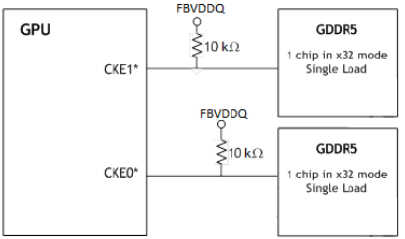


Figure 7-4. Clock Enable (CKE\*) Signal Connection, x32 Mode

### 7.1.7.3 RST\* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 kΩ pull-down resistor in standard mode or a clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

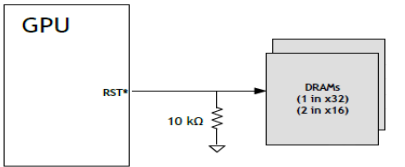


Figure 7-3. Reset Signal Connection

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μF	X7R	0402	2
		22 μF	X5R	0805	1
		Bead Type			
		30 Ω (ESR<0.010 Ω)	0603	1	Near GPU



# Memory Partition A

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128 Channel 0 0..31			GB2-64, GB2B-64, GB4B-128 Channel 1 32..63		
CMD0	C5*	CMD16	C5*		
CMD1	A3_BA3	CMD17	A3_BA3		
CMD2	A2_BA0	CMD18	A2_BA0		
CMD3	A4_BA2	CMD19	A4_BA2		
CMD4	A5_BA1	CMD20	A5_BA1		
CMD5	WE*	CMD21	WE*		
CMD6	A7_A8	CMD22	A7_A8		
CMD7	A6_A11	CMD23	A6_A11		
CMD8	AB1*	CMD24	AB1*		
CMD9	A12_RFU	CMD25	A12_RFU		
CMD10	A0_A10	CMD26	A0_A10		
CMD11	A1_A9	CMD27	A1_A9		
CMD12	RA5*	CMD28	RA5*		
CMD13	RST*	CMD29	RST*		
CMD14	CKE*	CMD30	CKE*		
CMD15	CAS*	CMD31	CAS*		

GB2-64, GB2B-64, GB4B-128 Channel 0 & 1		
CMD32	Not Used	
CMD33	Not Used	
CMD34	DEBUG2*	
CMD35	DEBUG1*	

Notes:  
1. Not available in GB2-64 and GB2B-64 packages.  
2. GPU debug pins not connected to UGAM; see section 7.1.13.

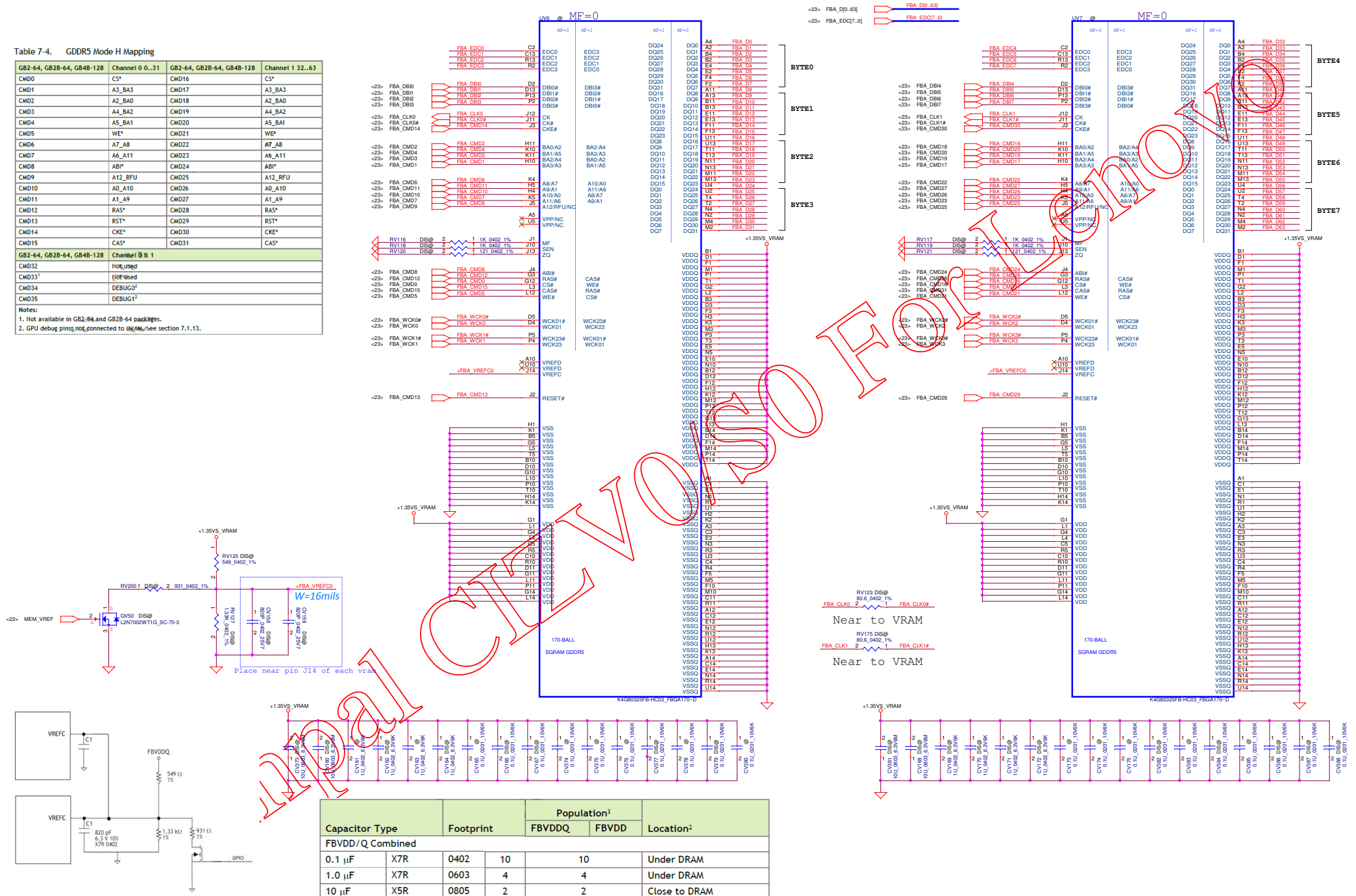
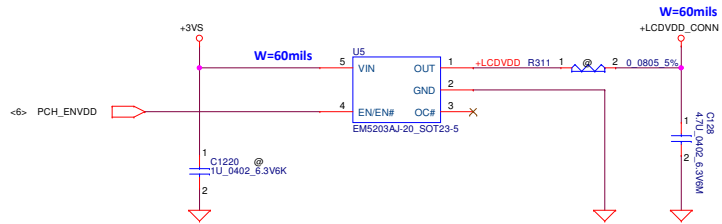


Figure 7-9. VREF-C Connections for x32 Mode

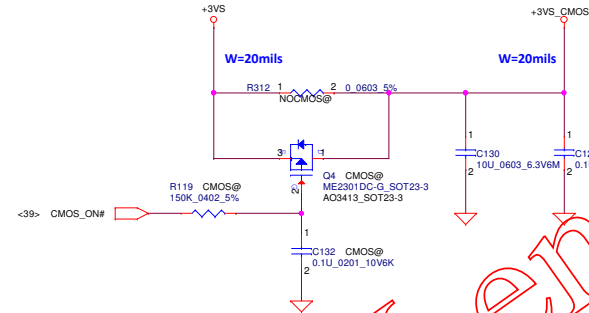
Capacitor Type	Footprint	Population <sup>1</sup>		Location <sup>2</sup>
		FBVDDQ	FBVDD	
FBVDD/Q Combined				
0.1 μF	X7R	0402	10	Under DRAM
1.0 μF	X7R	0603	4	Under DRAM
10 μF	X5R	0805	2	Close to DRAM

- Notes:
1. Per sub-partition, for example, per two pieces of x16 DRAM or one piece of x32 DRAM.
  2. Location is close to DRAM for all decoupling with x16 DRAM.

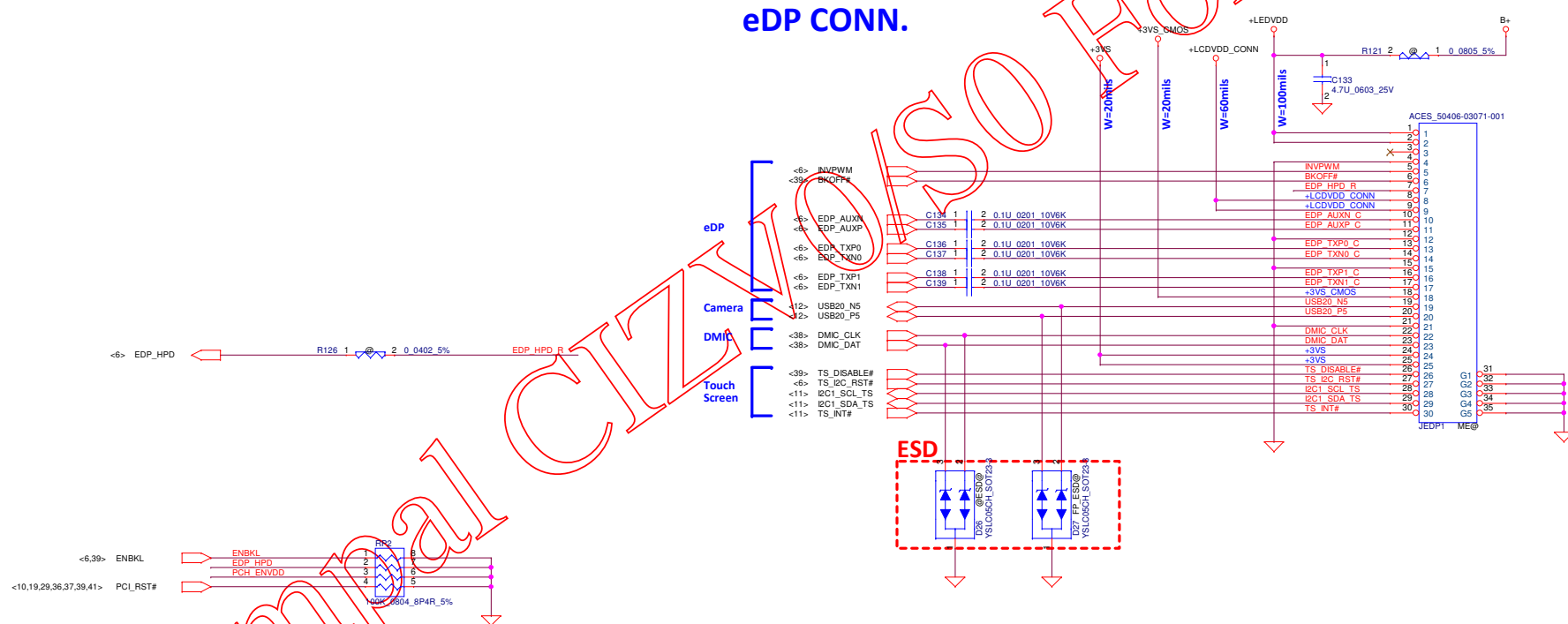
## LCD Power Circuit



## Camera

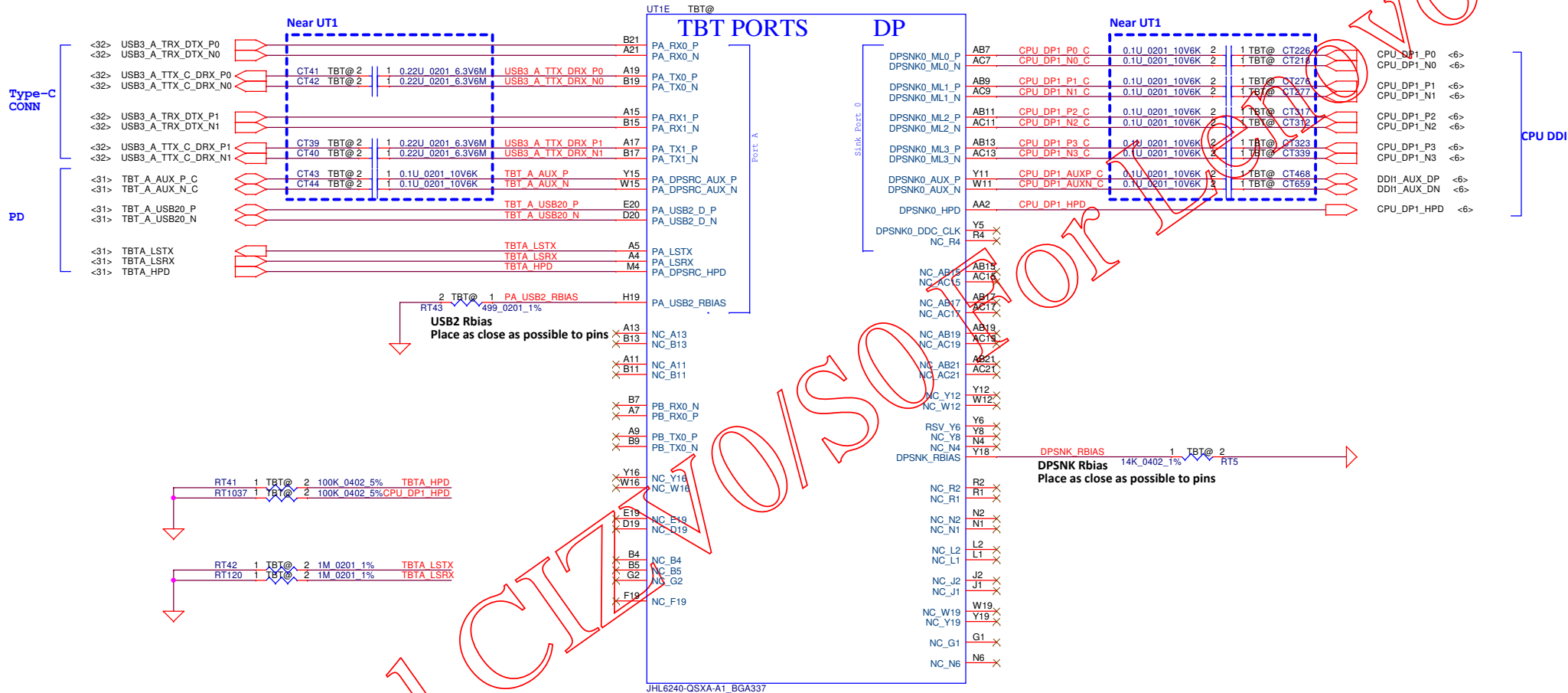


**eDP CONN.**



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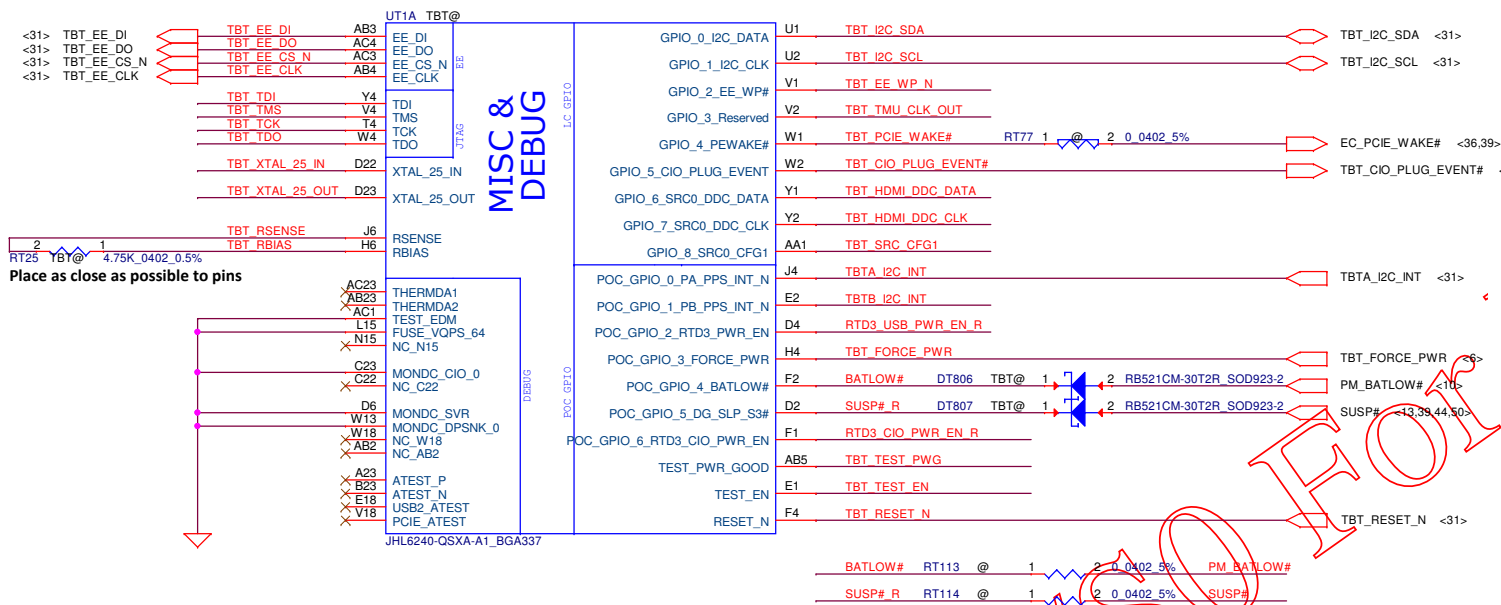
# Alpine Ridge LP - TBT, USB2 & DP Part



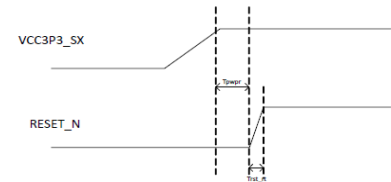
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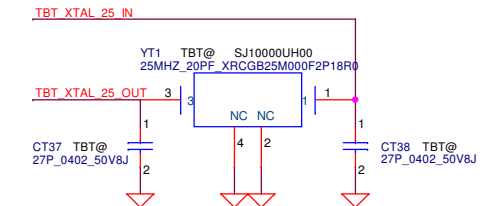
## Alpine Ridge LP - Misc Part



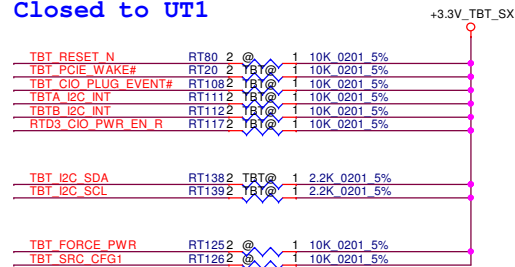
### Figure 72. Power On Sequence

**Table 422. Power On Sequence**

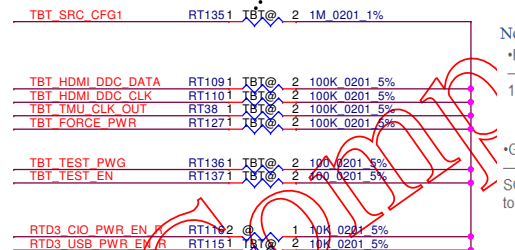
Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	



Closed to UT1



TBT\_SRC\_CFG1=0 for AUX, 1 for DDC  
If no SRC port, pls left open ,  
but put RBIAS 14K and HPD 100K pull down



Note: BIOS needs below GPIO.

- POC\_GPIO\_3 (TBT\_FORCE\_PWR)  
— Connects to a PCH GPIO and has  
100K ohm pull-down resistor to GND.

- GPIO\_5 (TBT\_CIO\_PLUG\_EVENT\_N) —Connect to PCH GPIO that support SCI# and has 3.3K ohm pull-up resistor to VCC3V3\_TBT\_SX power domain.

- GPIO\_3 (TBT\_PCl\_e\_WAKE\_N)  
—Connect to relevant PCl\_e wake signal and has 10K ohm pull-up resistor to VCC3V3 TBT\_SX power domain.

POC\_GPIO\_4 (BATLOW\_N)  
POC\_GPIO\_5 (SLP\_S3\_N)

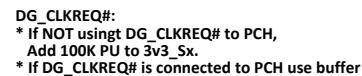
If no use : Reserve 10K ohm pull-up resistor to VCC3V3\_TBT\_SXpower domain.  
If use : Add buffer between AR and PCH

### Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
AMIC	A25L080	8.0	3.0-3.6
Spansion	S25FL208K	8.0	2.7-3.6
Winbond	W25Q80DV	8.0	2.7-3.6

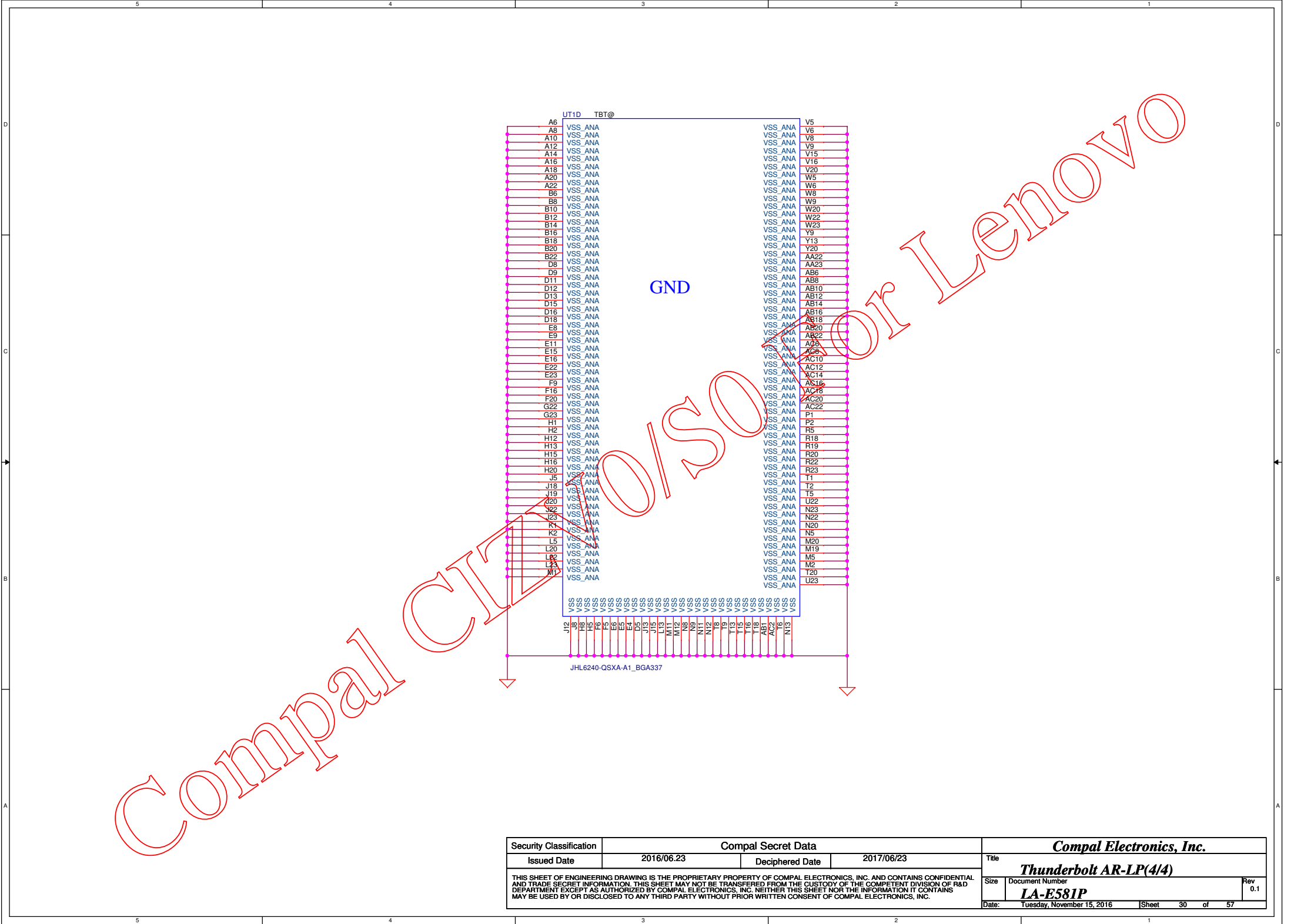
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### Table 423. External Power Supply Specification



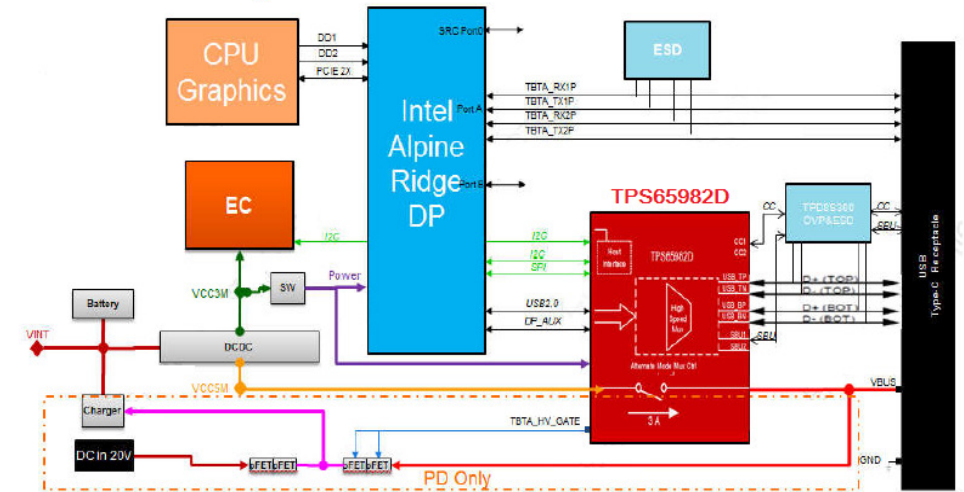
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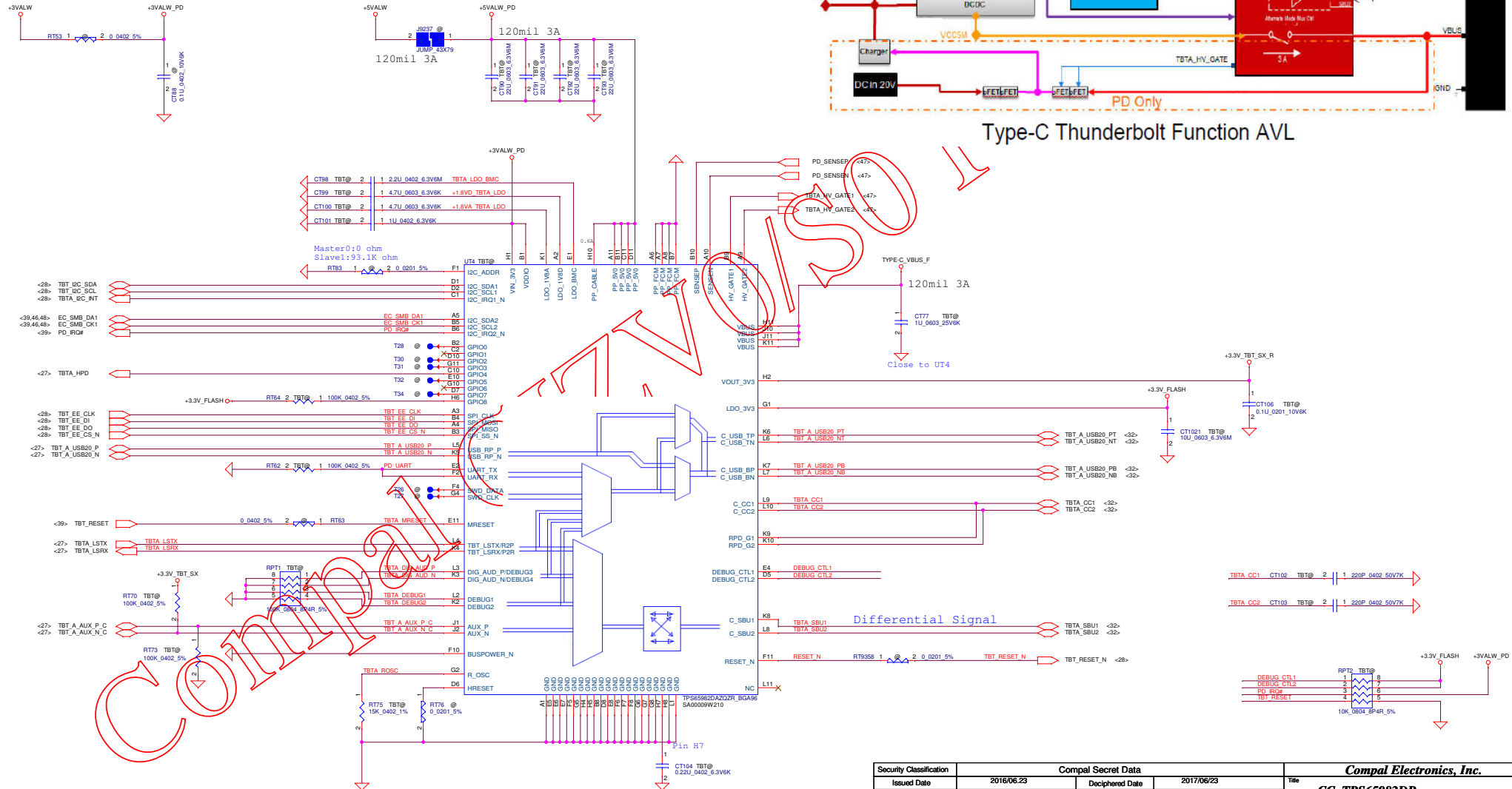


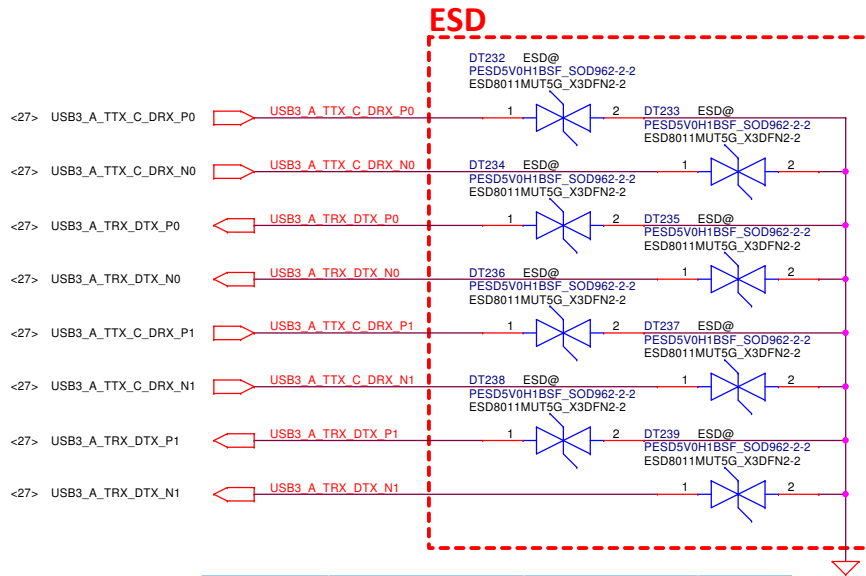
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				Size	Document Number	Rev
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# Type-C Thunderbolt Function Block Ref

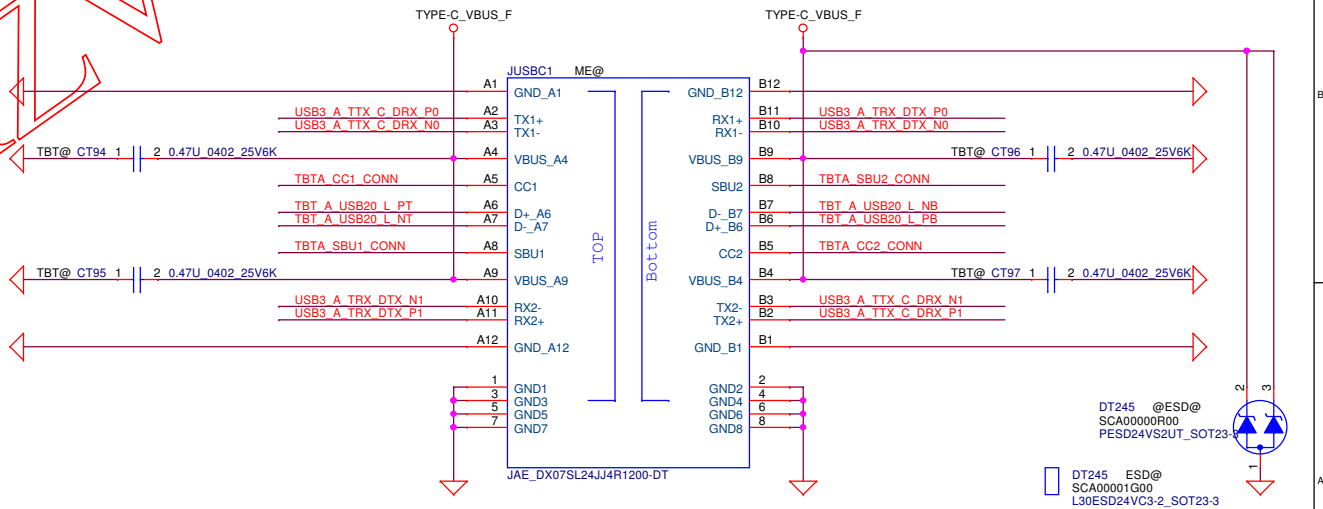
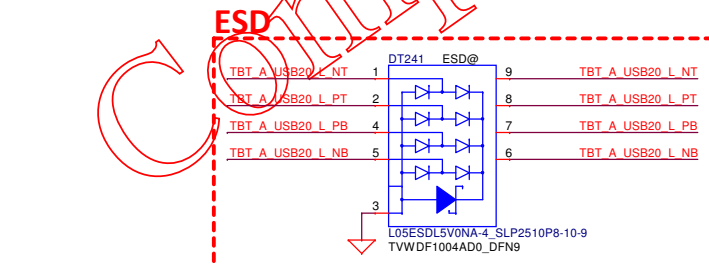
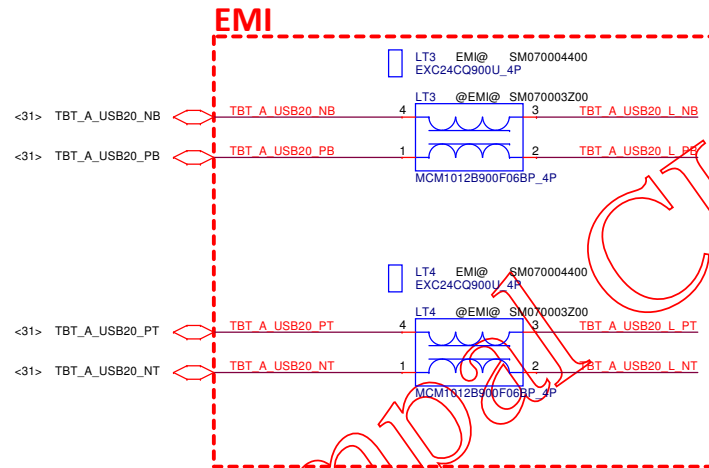
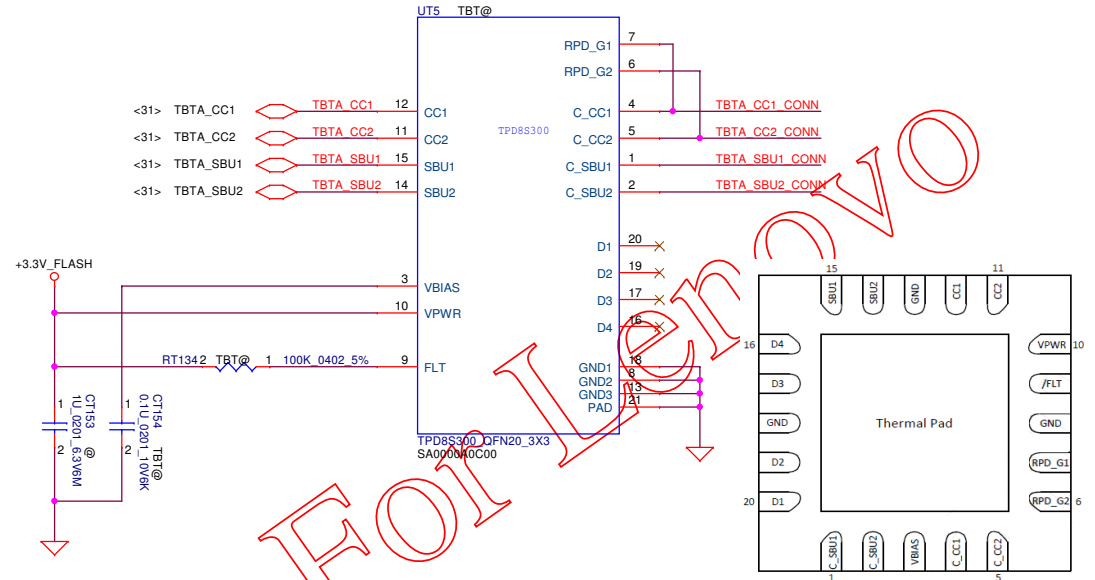


# Type-C Thunderbolt Function AVL

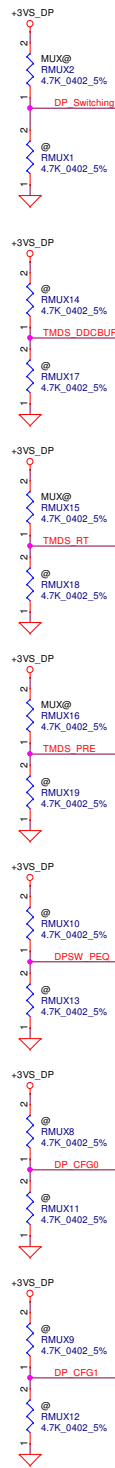




Manufacture	P/N	Capacitance @ 1MHz	Reverse Volta
Infinion	ESD101-B1-02EL	0.2pF	± 5.5v
Little-Fuse	SESD0201X1BN	0.13pF	± 7.0v
NXP	PESD5V0H1BSF	0.19pF	5.0v



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## HDMI first

DP_Switching	Function (For Automatic Switching)
* H	TMDS output has higher priority
L	DP output has higher priority

## DDC Pull High on CPU Side

TMDS_PRE	Function
H	DDC active buffer
M	DDC pass through with 40 kohm pull up resistor
L	DDC pass through

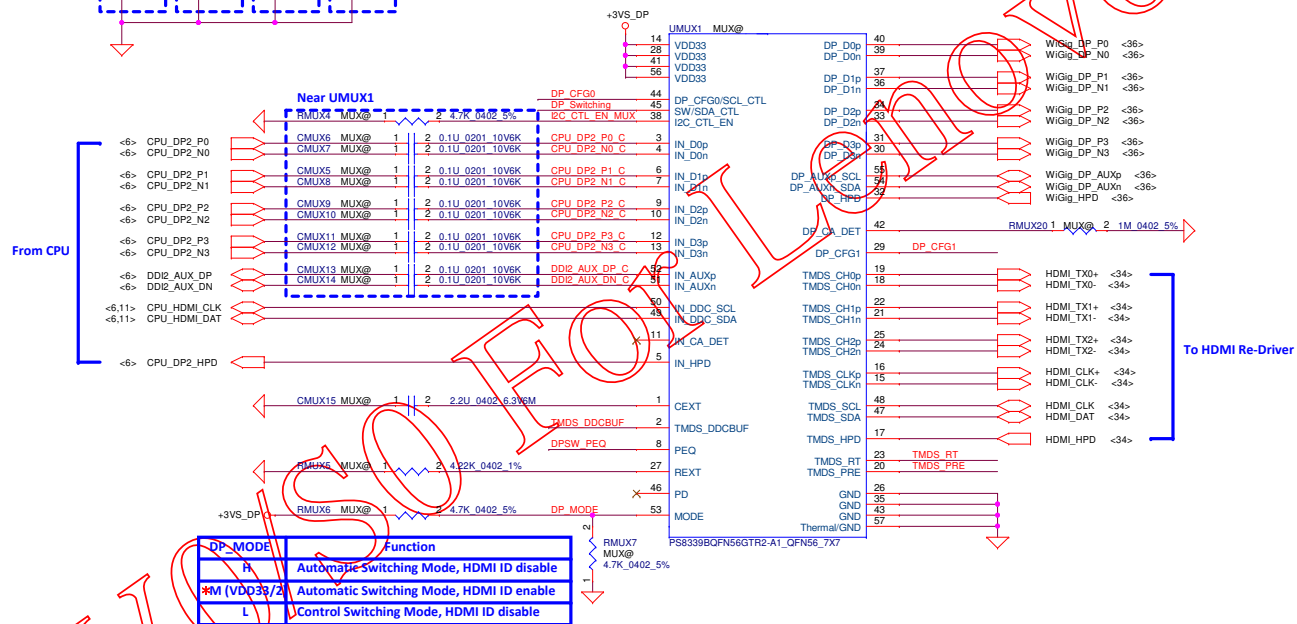
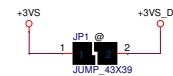
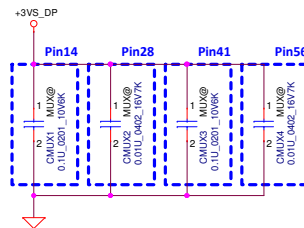
TMDS_RT	Function
H	Open drain driver with termination resistors
L	Standard open drain driver

TMDS_PRE	Function
H	1.5dB pre-emphasis
M	3.0dB pre-emphasis
L	no pre-emphasis

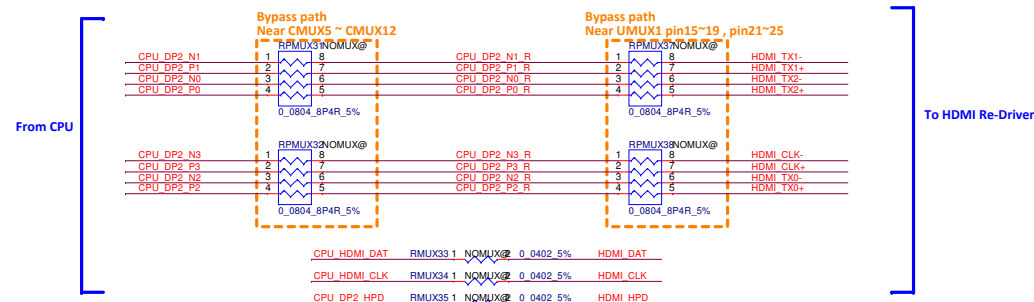
DPSW_PEQ	Function
H	HEQ, compensate channel loss up to 15dB @ HBR2
M	LLEQ, compensate channel loss up to 5dB @ HBR2
L	default, LEQ, compensate channel loss up to 12dB @ HBR2

DP_CFG0	Function
H	automatic EQ disable & AUX interception enable
M	automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
L	default, automatic EQ enable & AUX interception enable

DP_CFG1	Function
H	auto test enable & input offset cancellation enable
M	auto test disable & input offset cancellation disable
L	default, auto test disable & input offset cancellation enable

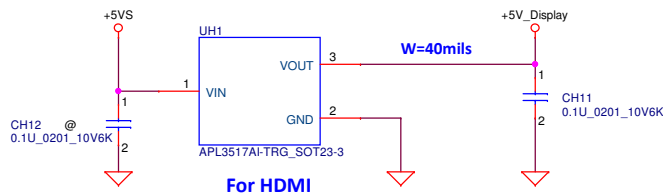


## For WLAN only

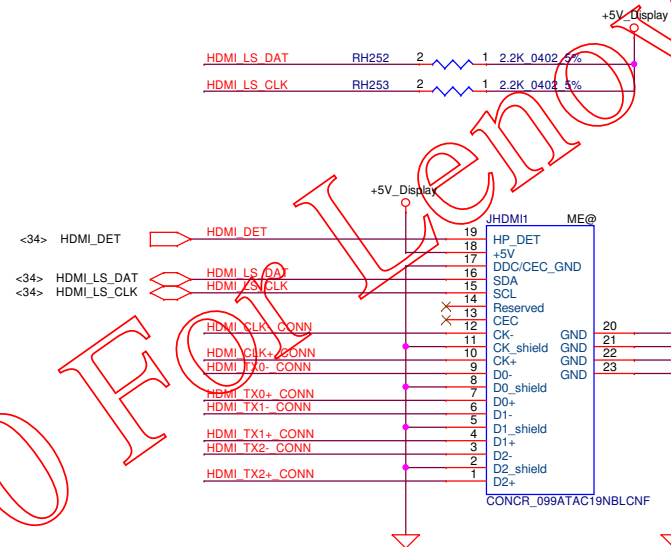
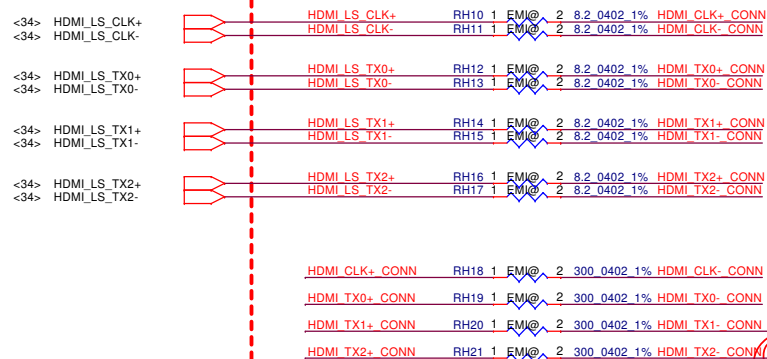


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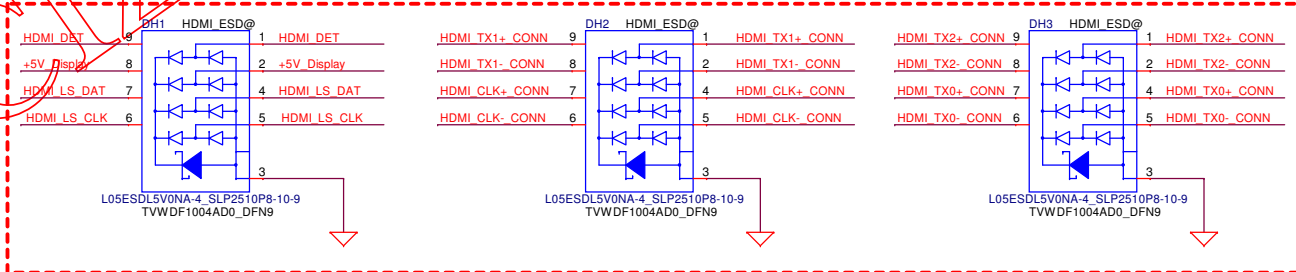




### EMI Near JHDMI1



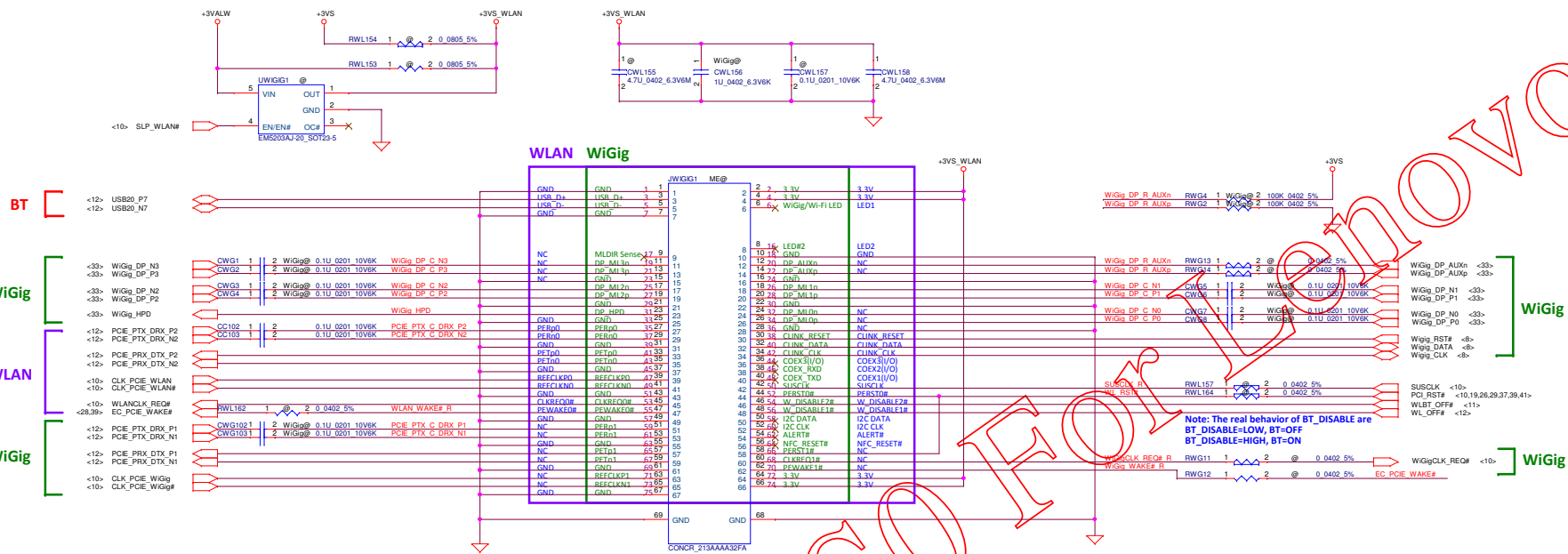
### ESD



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# NGFF for WiGig (Key A) , WLAN / BT(Key A-E)



## Intel 18265 WiGig / WLAN

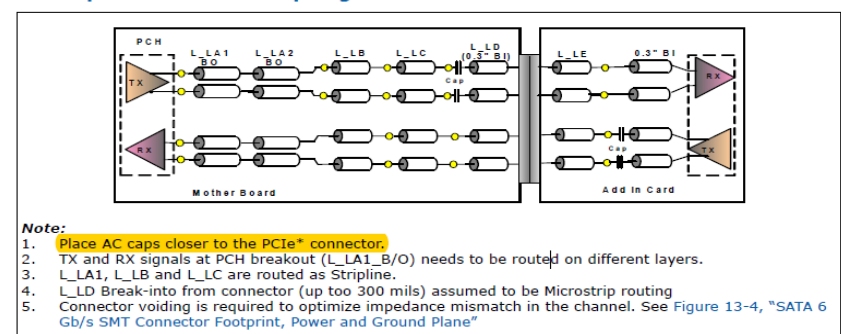
Pin #	Pin name platform pinout	Pin name module pinout	Voltage on and side	WLAN BT or BT/BT
1	GND	GND	3.3 V	All
2	USB_D+	USB_D+	3.3 V	BT
3	USB_D-	USB_D-	3.3 V	BT
4	USB_D+	USB_D+	3.3 V	BT
5	USB_D-	USB_D-	3.3 V	BT
6	WiGig/Wi-Fi LED	WiGig/Wi-Fi LED	3.3 V	WiGig+Wi-Fi
7	Connector Key	Connector Key		
8	Connector Key	Connector Key		
9	Connector Key	Connector Key		
10	Connector Key	Connector Key		
11	Connector Key	Connector Key		
12	Connector Key	Connector Key		
13	Connector Key	Connector Key		
14	Connector Key	Connector Key		
15	Connector Key	Connector Key		
16	LED2	LED2	3.3V	BT
17	MLDIR Sense (I)	DP_MLDIR GND (In)	3.3V	WiGig
18	GND	GND		
19	DP_ML3n	DP_ML3n	Display	WiGig
20	DP_AUXn	DP_AUXn	Display	WiGig
21	DP_ML3p	DP_ML3p	Display	WiGig
22	DP_AUXp	DP_AUXp	Display	WiGig
23	GND	GND		
24	DP_ML2n	DP_ML2n	Display	WiGig
25	DP_ML2p	DP_ML2p	Display	WiGig
26	DP_ML3n	DP_ML3n	Display	WiGig
27	DP_ML3p	DP_ML3p	Display	WiGig
28	DP_ML3p	DP_ML3p	Display	WiGig
29	GND	GND		
30	GND	GND		
31	DP_HPD (IO/0.3.3V)	DP_HPD (IO/0.3.3V)	3.3 V	WiGig
32	DP_ML3n	DP_ML3n	Display	WiGig
33	DP_ML3p	DP_ML3p	Display	WiGig
34	DP_ML3p	DP_ML3p	Display	WiGig
35	PERp0	PERp0	1.8V	WiGig
36	GND	GND		
37	PERn0	PERn0	1.8V	WiGig
38	CLINK_RESET (IO/0.3.3V)	CLINK_RESET (IO/0.3.3V)	3.3V	WiGig
39	GND	GND		
40	CLINK_DATA	CLINK_DATA	Clk PHY	WLAN
41	PERp0	PERp0	Clk PHY	WLAN
42	CLINK_CLK	CLINK_CLK	Clk PHY	WLAN
43	PERn0	PERn0	Clk PHY	WLAN
44	COEX3(I/O) (S/L-BV)	COEX3(I/O) (S/L-BV)	1.8 V	WLAN + BT
45	GND	GND		
46	COEX_RXD (IO/0.1.8V)	COEX_RXD (IO/0.1.8V)	1.8 V	WLAN + BT
47	REFCLKP	REFCLKP	1.8 V	WLAN + BT
48	COEX_TXD (IO/0.1.8V)	COEX_TXD (IO/0.1.8V)	1.8 V	WLAN + BT
49	REFCLKN	REFCLKN	1.8 V	WLAN + BT
50	SUSCLK (IO/0.3.3 V)	SUSCLK (IO/0.3.3 V)	3.3 V	WiGig
51	GND	GND		
52	PERST# (IO/0.3.3V)	PERST# (IO/0.3.3V)	3.3 V	WLAN
53	CLINK_RESET (IO/0.3.3V)	CLINK_RESET (IO/0.3.3V)	3.3 V	BT
54	W_DISABLE# (IO/0.3.3V)	W_DISABLE# (IO/0.3.3V)	3.3 V	WLAN
55	W_DISABLE# (IO/0.3.3V)	W_DISABLE# (IO/0.3.3V)	3.3 V	WLAN
56	W_DISABLE# (IO/0.3.3V)	W_DISABLE# (IO/0.3.3V)	3.3 V	WLAN
57	GND	GND		
58	I2C DATA (IO/UART_RX (IO/0.1.8V)	I2C DATA (IO/UART_RX (IO/0.1.8V)	1.8 V	WLAN + BT
59	PERST#	PERST#	1.8 V	WLAN + BT
60	I2C CLK/UART_TX (IO/0.1.8V)	I2C CLK/UART_TX (IO/0.1.8V)	1.8 V	WLAN + BT
61	PERn0	PERn0	1.8 V	WLAN + BT
62	ALERT#/UART_RTS (IO/0.1.8V)	ALERT#/UART_RTS (IO/0.1.8V)	1.8 V	WLAN + BT
63	GND	GND		
64	NFC_RESET#/UART_CTS (IO/0.1.8V)	NFC_RESET#/UART_CTS (IO/0.1.8V)	1.8 V	WLAN + BT
65	PERST#	PERST#	1.8 V	WLAN + BT
66	PERST# (IO/0.3.3V)	PERST# (IO/0.3.3V)	3.3 V	WLAN
67	PERn0	PERn0	3.3 V	WLAN
68	CLINK_RESET (IO/0.3.3V)	CLINK_RESET (IO/0.3.3V)	3.3 V	WLAN
69	GND	GND		
70	PERAKE# (IO/0.3.3V)	PERAKE# (IO/0.3.3V)	3.3 V	WLAN
71	REFCLKP	REFCLKP	3.3 V	WLAN
72	REFCLKN	REFCLKN	3.3 V	WLAN
73	REFCLKP	REFCLKP	3.3 V	WLAN
74	REFCLKN	REFCLKN	3.3 V	WLAN
75	GND	GND		

## Athros NFA344A WLAN

### PIN ASSIGNMENT(MODULE KEY A-E)

Pin	Pin Define	Status	Pin	Pin Define	Status
1	GND	YES	2	3.3V	YES
3	USB_D+	YES	4	3.3V	YES
5	USB_D-	YES	6	LED_WLAN#	YES
7	GND	YES	8	NOTCH	NC
9	NOTCH	NC	10	NOTCH	NC
11	NOTCH	NC	12	NOTCH	NC
13	NOTCH	NC	14	NOTCH	NC
15	NOTCH	NC	16	LED_BT#	YES
17	NC	NC	18	GND	YES
19	NC	NC	20	NC	NC
21	NC	NC	22	NC	NC
23	NC	NC	24	NOTCH	NC
25	NOTCH	NC	26	NOTCH	NC
27	NOTCH	NC	28	NOTCH	NC
29	NOTCH	NC	30	NOTCH	NC
31	NOTCH	NC	32	NC	NC
33	GND	YES	34	NC	NC
35	PERp0	YES	36	NC	NC
37	PERn0	YES	38	RESERVED	NC
39	GND	YES	40	RESERVED	NC
41	PETp0	YES	42	RESERVED	NC
43	PETn0	YES	44	COEN3 (LTE_ACTIVE)	YES
45	GND	YES	46	COEN2 (LTE_PR)	YES
47	REFCLK+	YES	48	COEN1 (LITE_SYNC)	YES
49	REFCLK-	YES	50	SUSCLK(32kHz)	NC
51	GND	YES	52	PERST#	YES
53	CLKREQ#	YES	54	BT_DISABLE#	YES
55	PEWAKE#	YES	56	W_DISABLE#	YES
57	GND	YES	58	I2C DATA	NC
59	RESERVED	NC	60	I2C CLK	NC
61	RESERVED	NC	62	ALERT	NC
63	GND	YES	64	RESERVED	NC
65	RESERVED	NC	66	RESERVED	NC
67	RESERVED	NC	68	RESERVED	NC
69	GND	YES	70	RESERVED	NC
71	RESERVED	NC	72	3.3V	Yes
73	RESERVED	NC	74	3.3V	Yes
75	GND	YES			

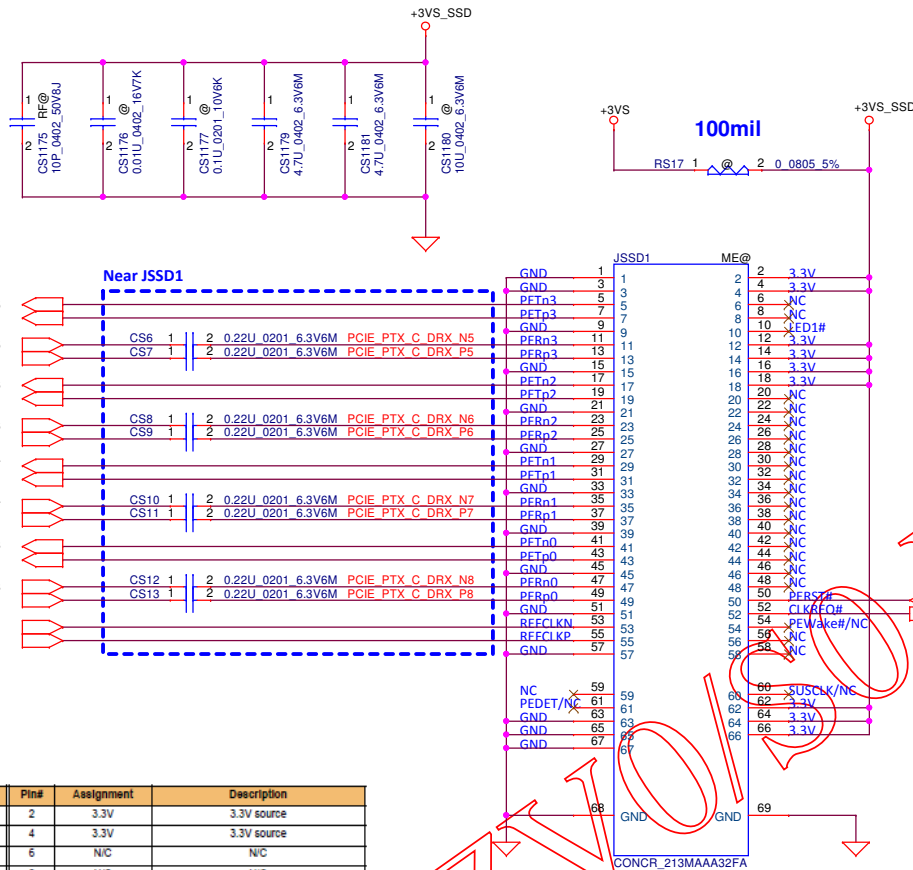
## PCI Express\* Interface Topologies on the Motherboard



- Note:**
- Place AC caps closer to the PCIe\* connector.
  - TX and RX signals at PCH breakout (L\_LA1\_B/O) needs to be routed on different layers.
  - L\_LA1, L\_LB and L\_LC are routed as Stripline.
  - L\_LD Break-into from connector (up too 300 mils) assumed to be Microstrip routing
  - Connector voiding is required to optimize impedance mismatch in the channel. See Figure 13-4, "SATA 6 Gb/s SMT Connector Footprint, Power and Ground Plane"



# SSD(Key M)



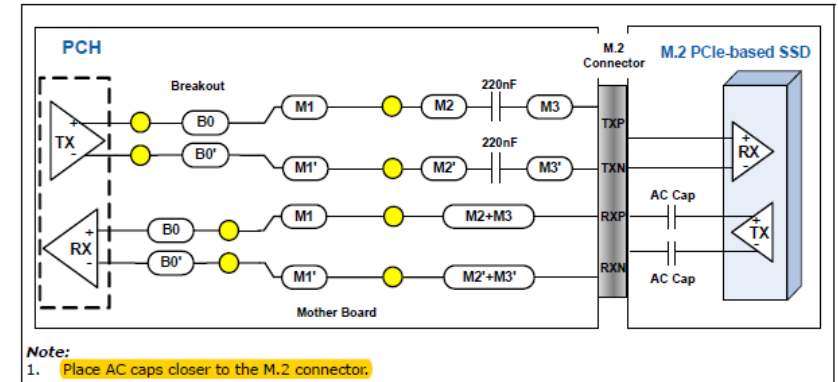
SSD PCIE

## 4.2 Pin Assignments and Definition

[Table 10] Signal Assignments

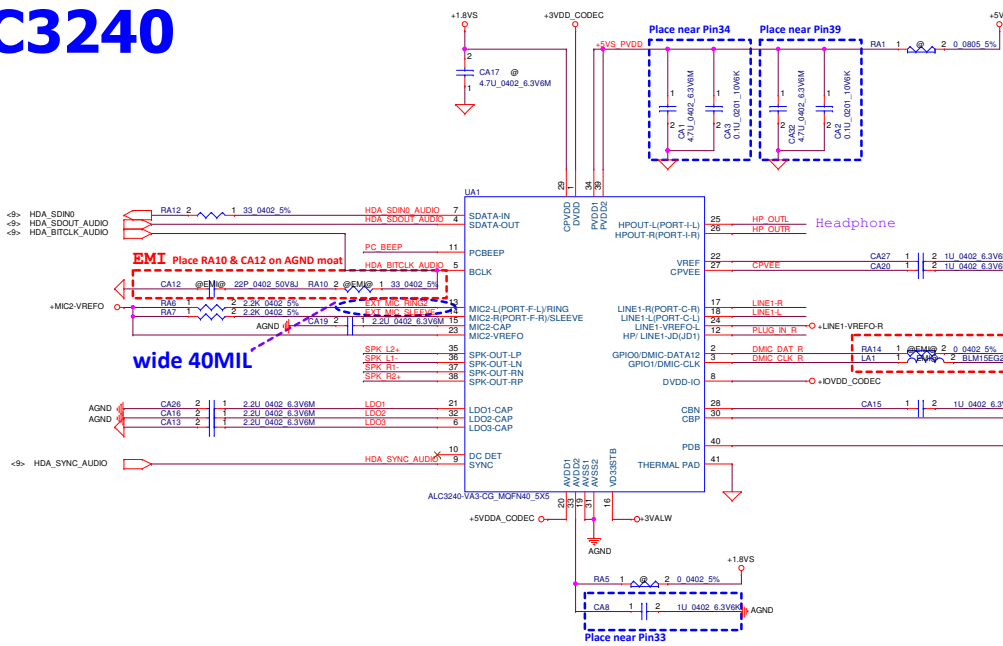
Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCie TX	6	N/C	N/C
7	PETp3	PCie TX	8	N/C	N/C
9	GND	Return current path	10	LED1#	Device Active Signal
11	PERn3	PCie Rx	12	3.3V	3.3V source
13	PERp3	PCie Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCie TX	18	3.3V	3.3V source
19	PETp2	PCie TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCie Rx	24	N/C	N/C
25	PERp2	PCie Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCie TX	30	N/C	N/C
31	PETp1	PCie TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCie Rx	36	N/C	N/C
37	PERp1	PCie Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCie TX	42	N/C	N/C
43	PETp0	PCie TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCie Rx	48	N/C	N/C
49	PERp0	PCie Rx	50	PERST#	PCie Reset
51	GND	Return current path	52	CLKREQ#	PCie Device Clock Request
53	REFCLKN	PCie Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCie Reference Clock	56	N/C	N/C
57	GND	Return current path	58	N/C	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

## PCI Express\* Topology Routing Guidelines on the Motherboard for M.2 SSD Modules

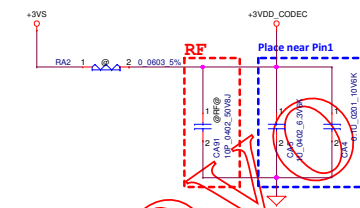


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				Date:	Tuesday, November 15, 2016	ISheet

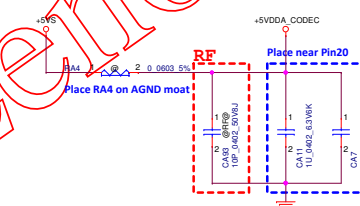
# ALC3240



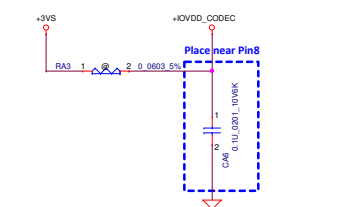
## +3VS → +3VDD\_CODEC



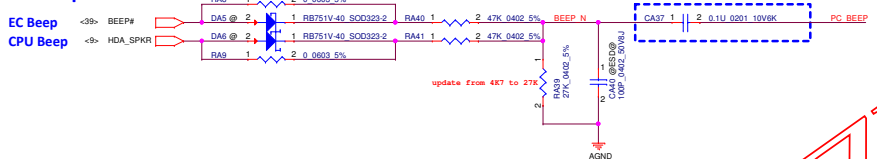
## +5VS → +5VDDA\_CODEC



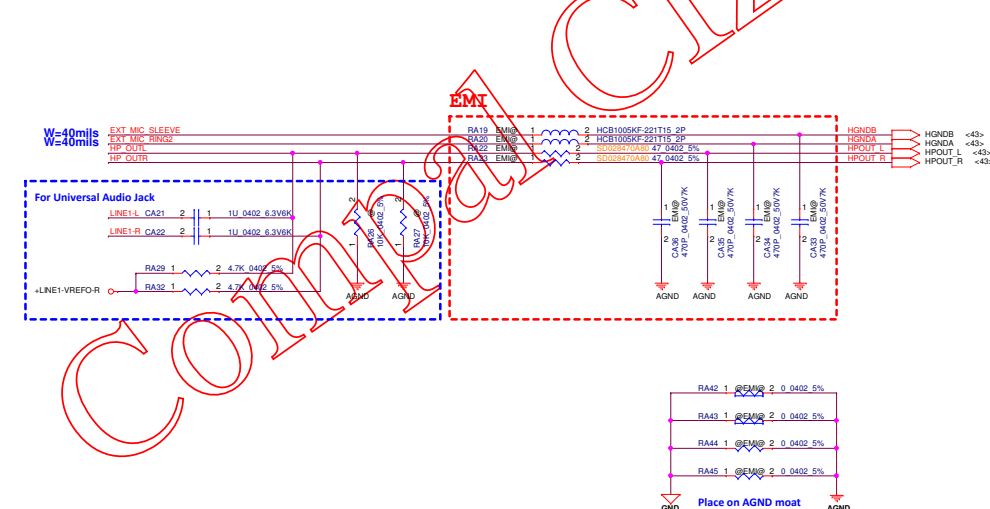
## +3VS → +IOVDD\_CODEC



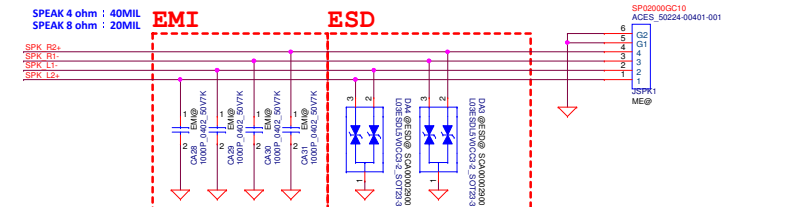
## PC BEEP



## Audio Combo Jack

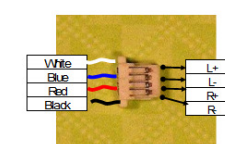


## Speaker



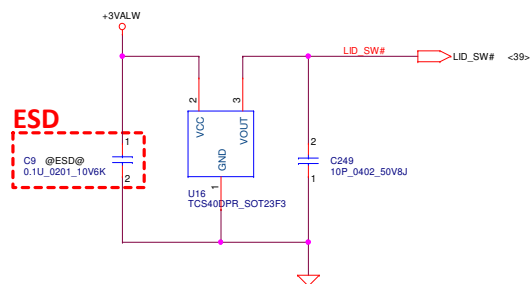
Note:

Cable Color	Pin Definition
A White	L+
B Blue	L-
C Red	R+
D Black	R-

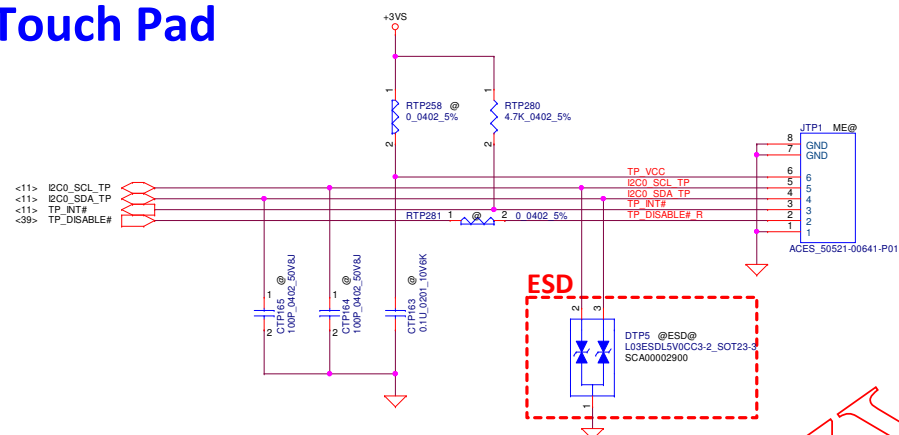




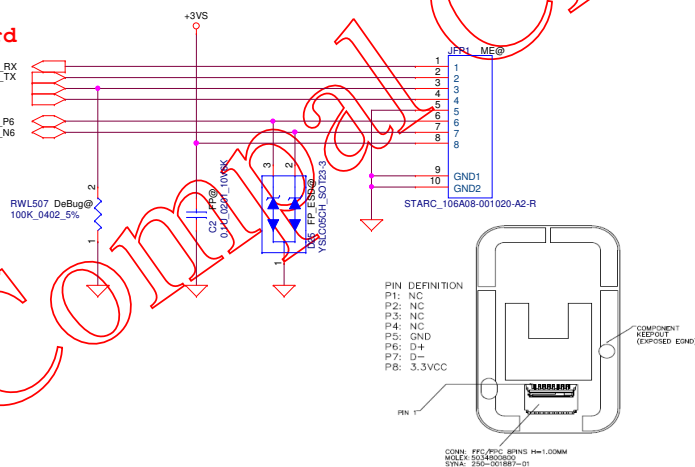
## LID Switch



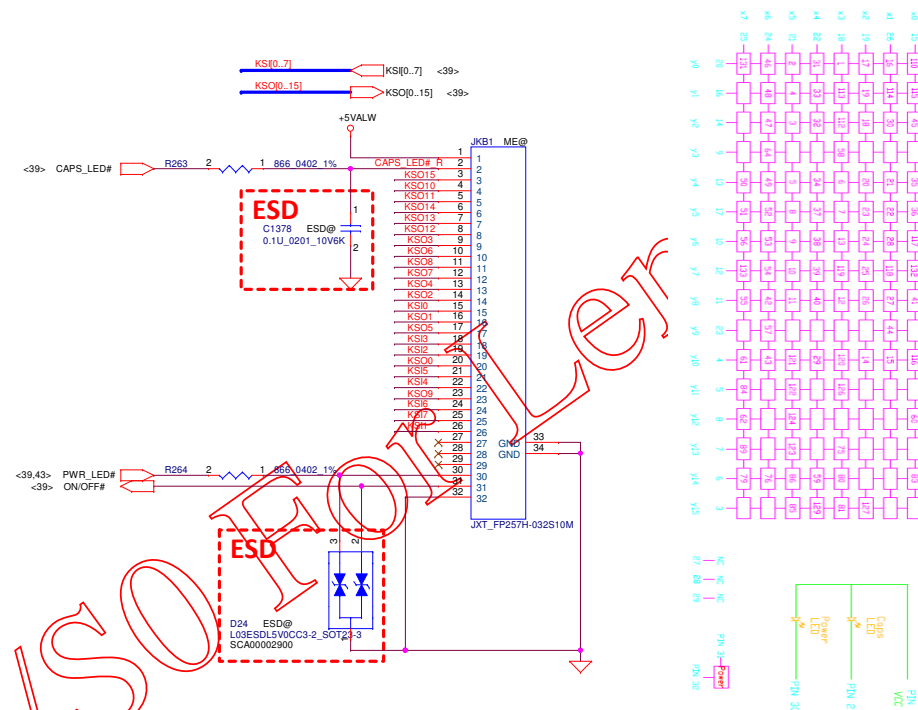
## Touch Pad



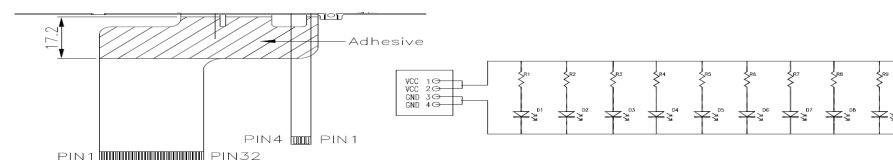
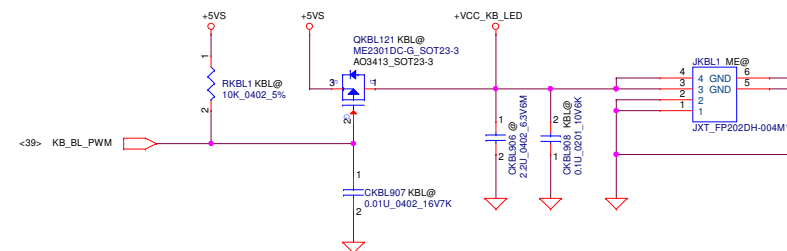
## Finger Print



## Keyboard

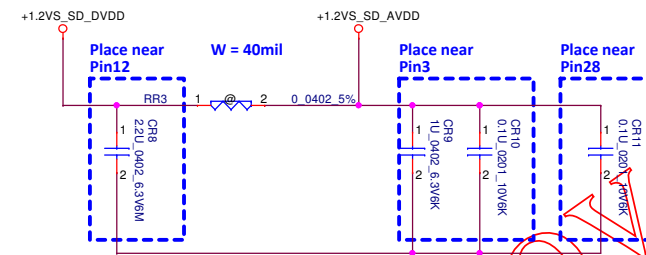
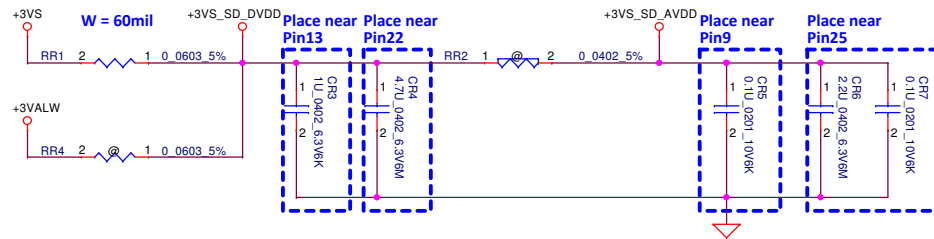


# Keyboard Backlight



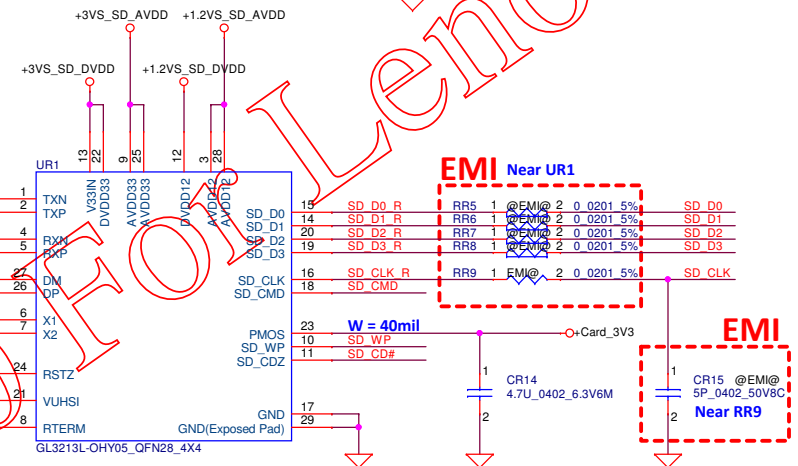
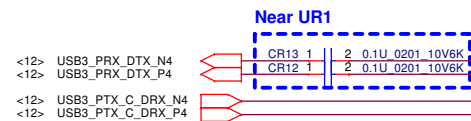
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						LID/TP/KB/KBL				
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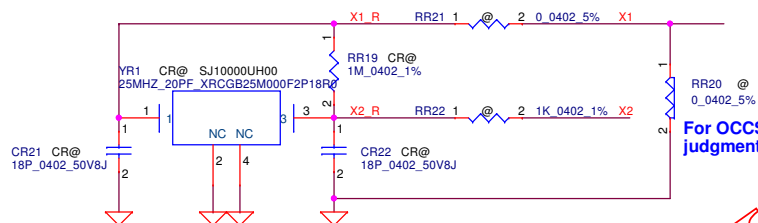


### For SS-only

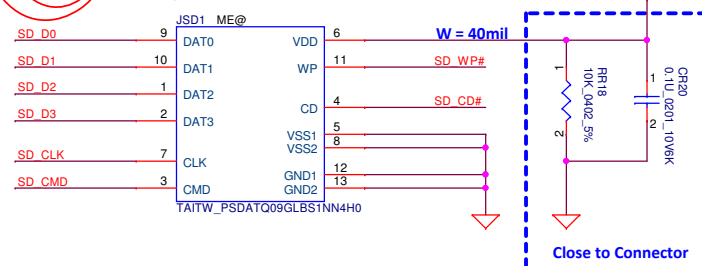
In the special case that a USB 3.0 device that does not require support for a USB 2.0 speed is used as an internal motherboard down device, it is possible to route only the SuperSpeed signals to this device as allowed by the USB 3.0 specification. In this special case, USB 2.0 and USB 3.0 signals will not need to be paired together.



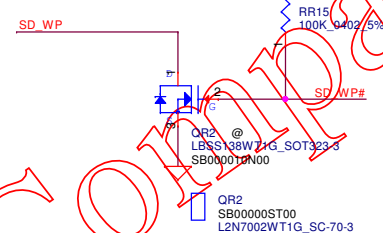
SD_CDZ	11	I, pu	SD card detect 0: Card insert 1: No card
SD_WP	10	I, pu	SD write protect 0: write enable 1: write protection



### SD/SDXC connector



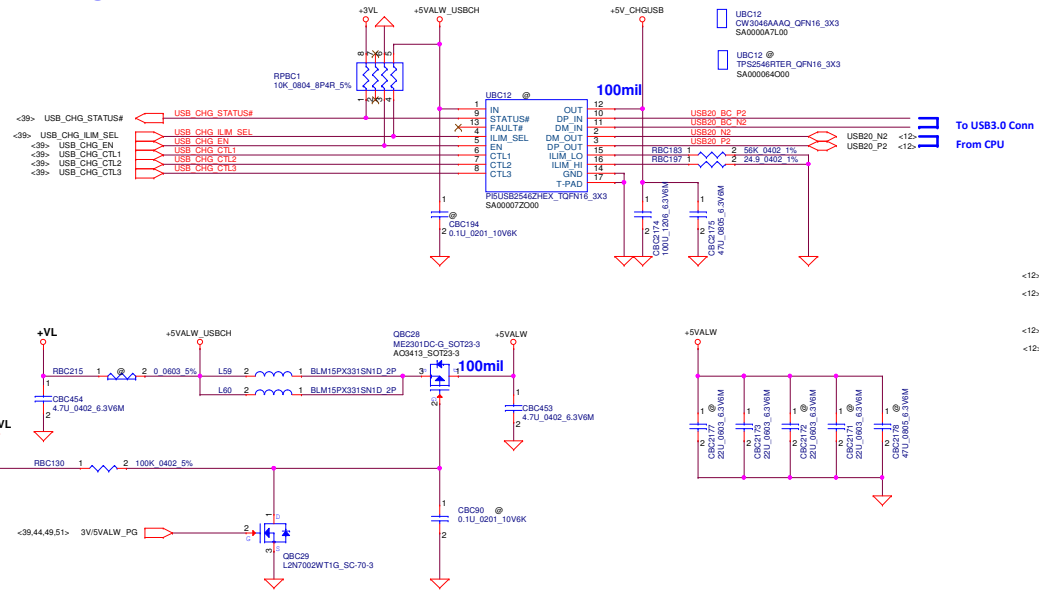
### W/P normal close Need Inverter



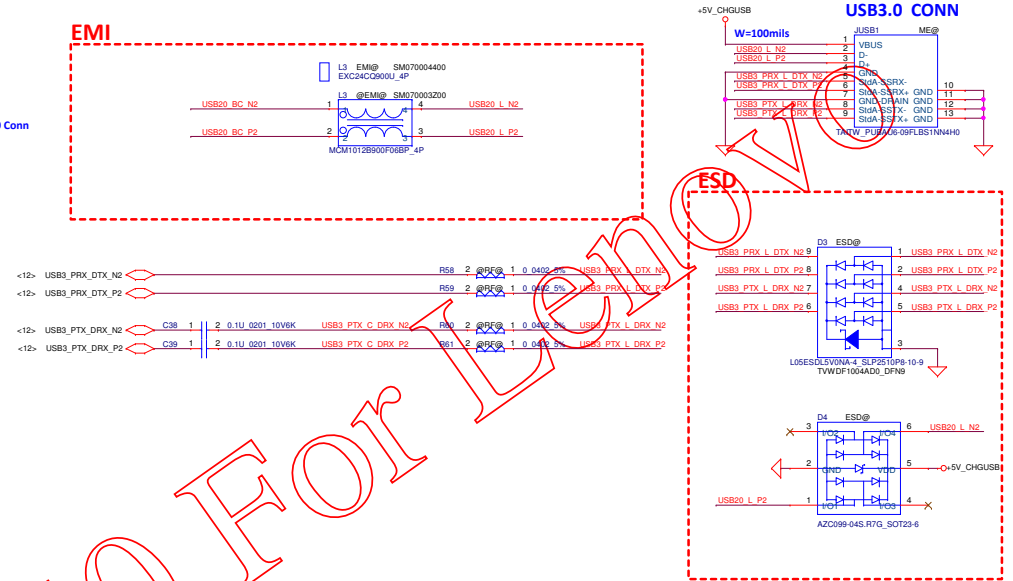
WITHOUT CARD	CARD INSERTED:LOCK	CARD INSERTED:UNLOCK
W/P GND	W/P GND	W/P GND
C/D VSS1 P3	C/D VSS1 P3	C/D VSS1 P3



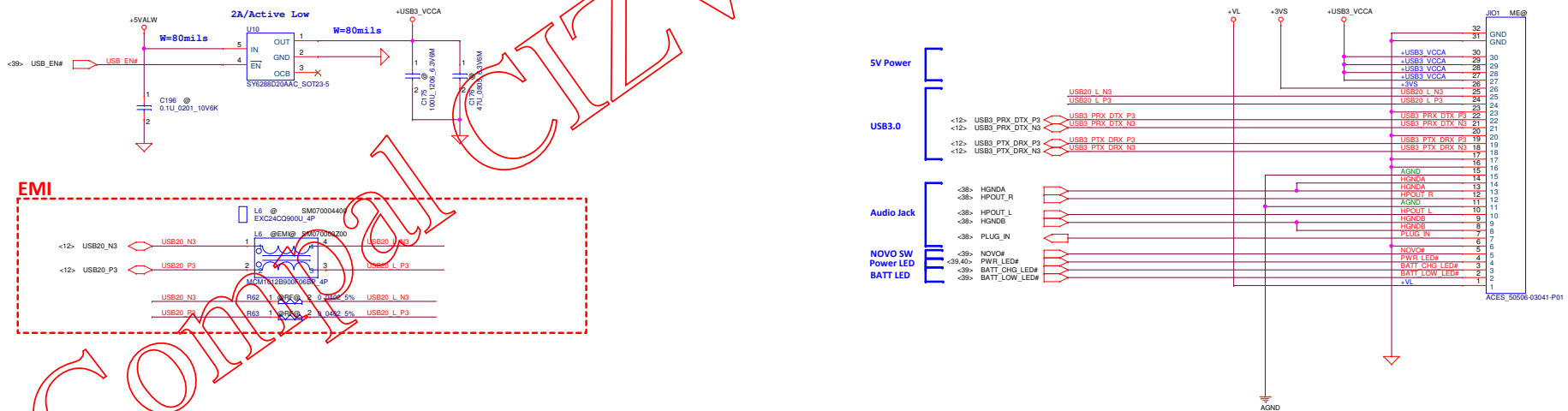
## USB Charge



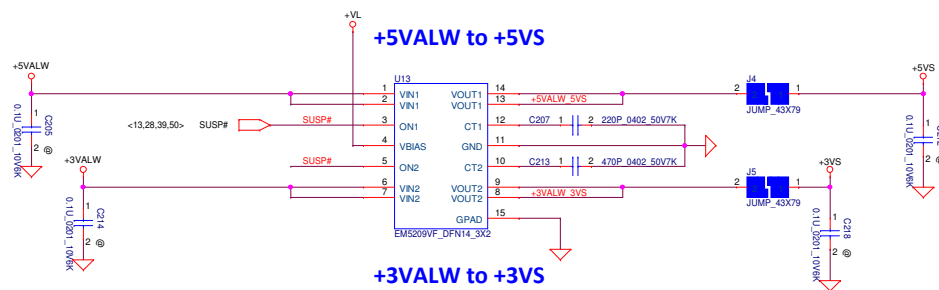
## USB3.0\_Port



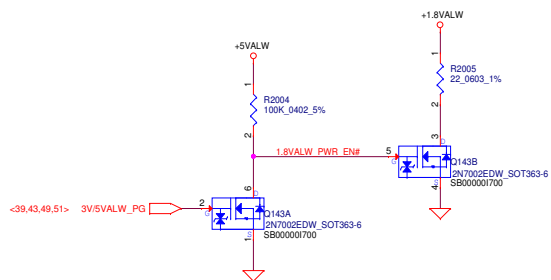
**To I/O Board**



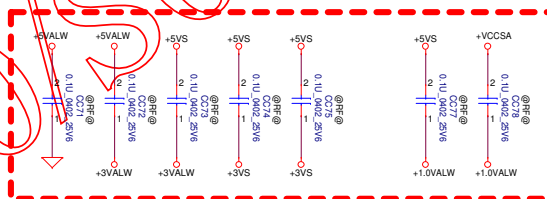
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Issued Date	2016/06/23	Deciphered Date	2017/06/23	<b>USB3 / IO Board</b> <b>LA-E581P</b>		
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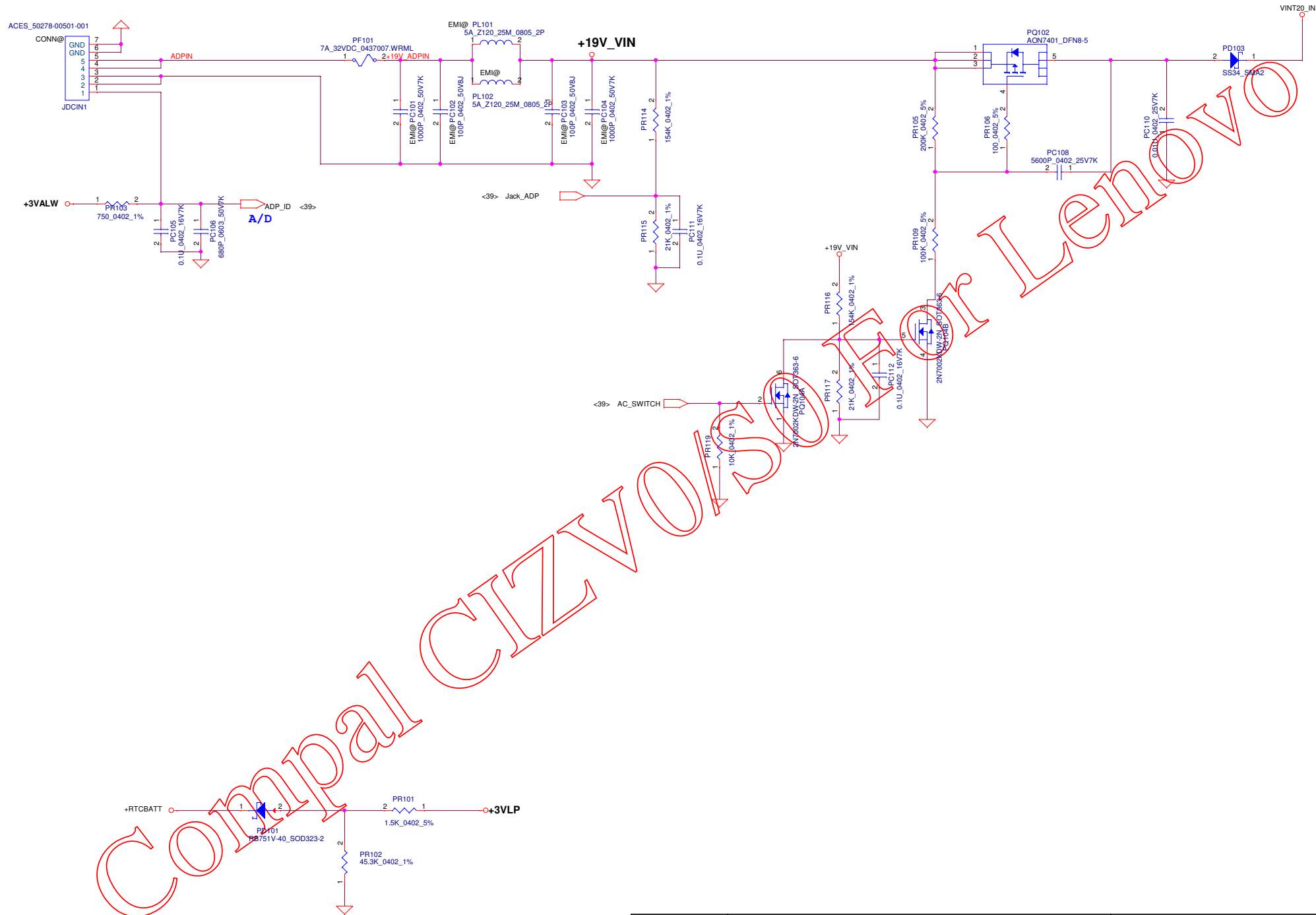
For +1.8VALW Discharge



For RF team request



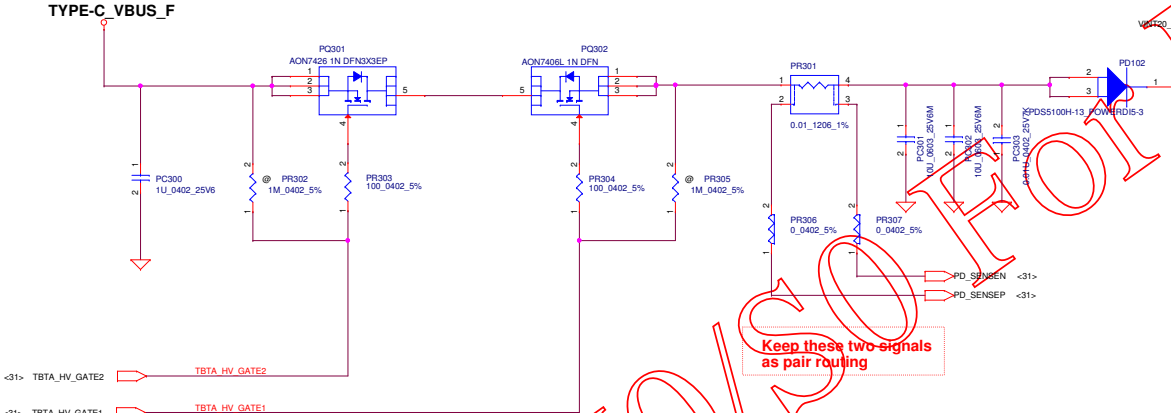
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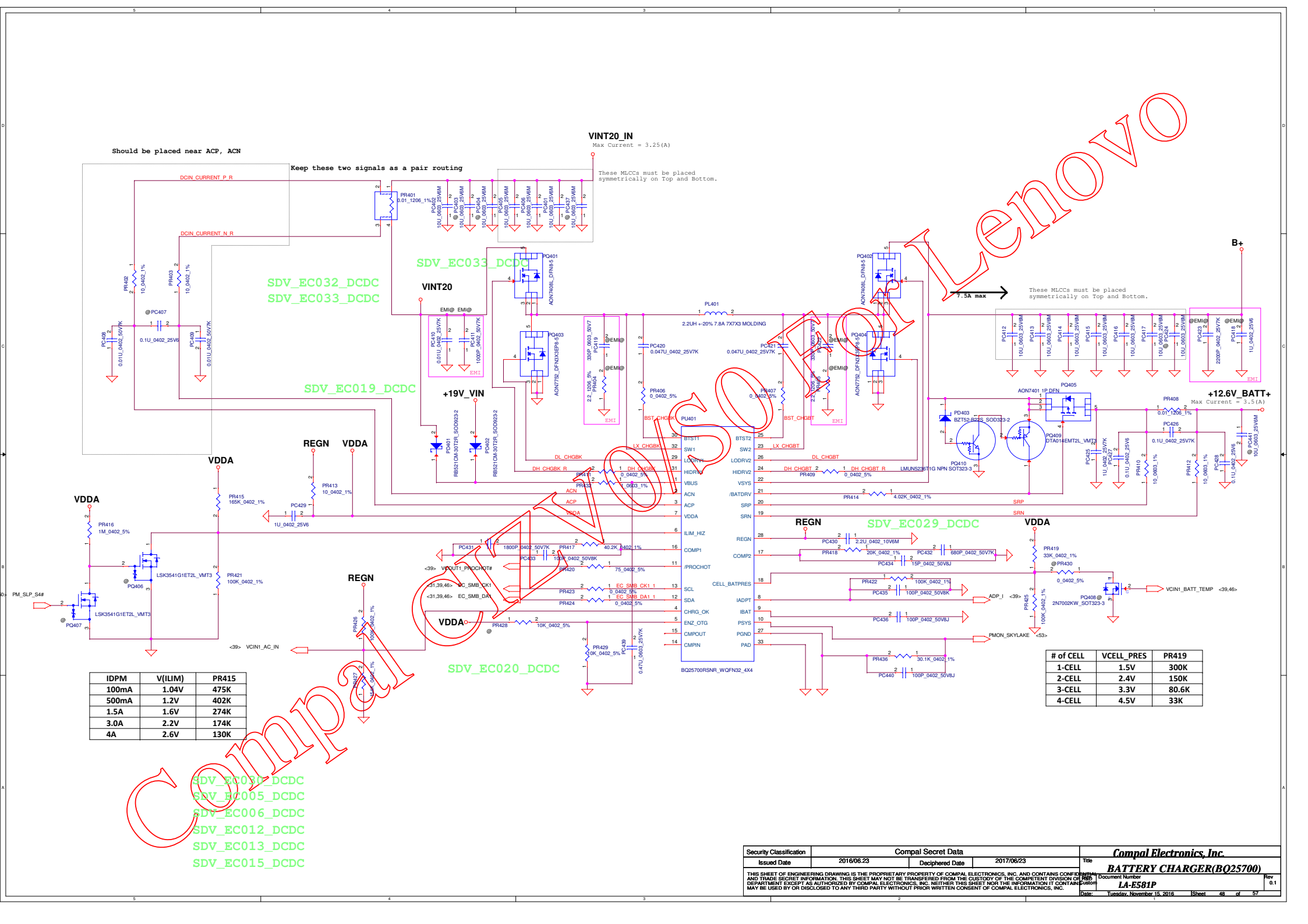
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## SDV\_EC022\_DCDC



Keep these two signals as pair routing



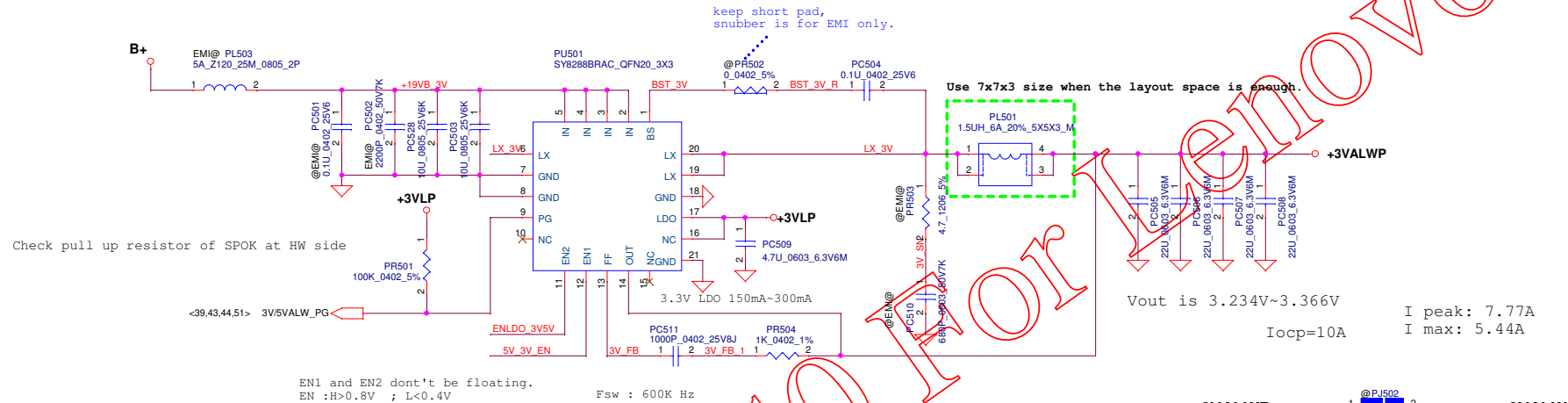
IDPM	V(ILIM)	PR415
100mA	1.04V	475K
500mA	1.2V	402K
1.5A	1.6V	274K
3.0A	2.2V	174K
4A	2.6V	130K

# of CELL	VCELL_PRES	PR419
1-CELL	1.5V	300K
2-CELL	2.4V	150K
3-CELL	3.3V	80.6K
4-CELL	4.5V	33K



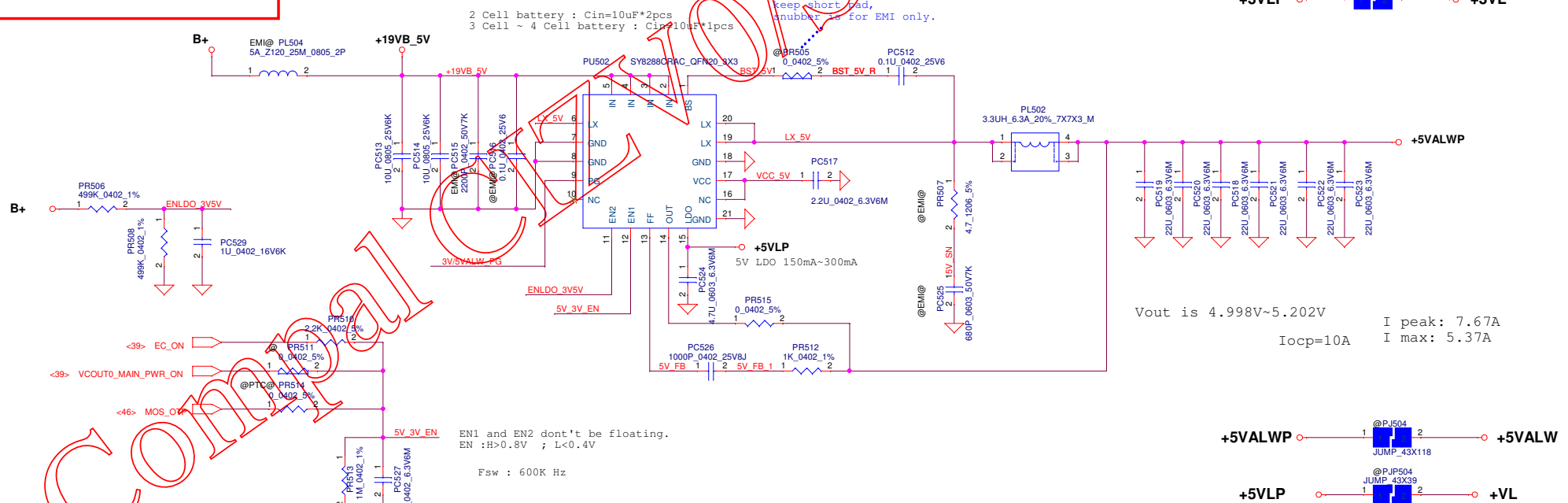
# Module model information

SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd



# Module model information

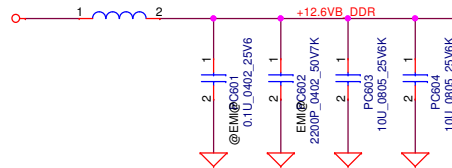
SY8286C\_V3\_single.mdd  
SY8286C\_V3\_dual.mdd



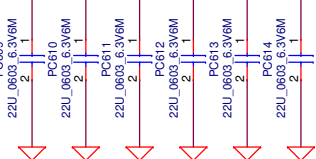
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				Date: Tuesday, November 15, 2016 Sheet 49 of 57

EMI@ PL601  
5A\_Z120\_25M\_0805\_2P

B+



+1.2VP



MOSFET: 3x3 DFN  
H/S Rds (on) : 27mohm (Typ) , 34mohm (Max)  
Idsm : 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on) : 19mohm (Typ) , 23.5mohm (Max)  
Idsm : 11A@Ta=25C, 8.8A@Ta=70C

Choke: 7x7x3  
Rdc=6.7mohm (Typ) , 7.4mohm (Max)

Switching Frequency:540kHz  
Ipeak=8A  
Iocp~9.6A  
OVP: 113%~120%  
VFB=0.75V, Vout=1.3545V

Mode Level +0.675VSP VTTREF\_1.35V  
S5 L off off  
S3 L off on  
S0 H on on  
Note: S3 - sleep ; S5 - power off

+3VALW

+5VALW

JUMP\_43X79  
@ PJ603

PC620  
1U\_0402\_6.3V6K

PC621  
4.7U\_0603\_6.3V6K

PC622  
1U\_0402\_16V7K

PC623  
1U\_0402\_16V7K

PC624  
22U\_0603\_6.3V6M

PC625  
1U\_0402\_16V7K

PC626  
1U\_0402\_16V7K

PC627  
1U\_0402\_16V7K

PC628  
1U\_0402\_16V7K

PC629  
1U\_0402\_16V7K

PC630  
1U\_0402\_16V7K

PC631  
1U\_0402\_16V7K

PC632  
1U\_0402\_16V7K

PC633  
1U\_0402\_16V7K

PC634  
1U\_0402\_16V7K

PC635  
1U\_0402\_16V7K

PC636  
1U\_0402\_16V7K

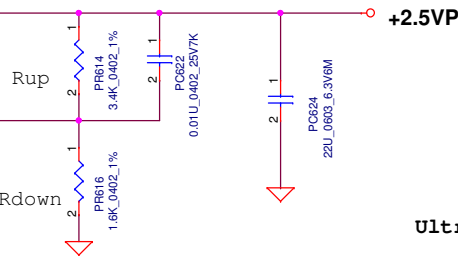
PC637  
1U\_0402\_16V7K

PC638  
1U\_0402\_16V7K

PC639  
1U\_0402\_16V7K

PC640  
1U\_0402\_16V7K

Vout=0.8V\* (1+Rup/Rdown)



Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675VOLT +/- 5%  
TDC 0.7A  
Peak Current 1A

+1.2VP

+0.6VSP

+1.2VP

6.04K\_0402\_1%

PR607

PR609

10K\_0402\_1%

PR610

0.0402\_5%

PR611

0.0402\_5%

PR612

0.0402\_5%

PR613

0.0402\_5%

PR614

0.0402\_5%

PR615

0.0402\_5%

PR616

0.0402\_5%

PR617

0.0402\_5%

PR618

0.0402\_5%

PR619

0.0402\_5%

PR620

0.0402\_5%

PR621

0.0402\_5%

PR622

0.0402\_5%

PR623

0.0402\_5%

PR624

0.0402\_5%

PR625

0.0402\_5%

PR626

0.0402\_5%

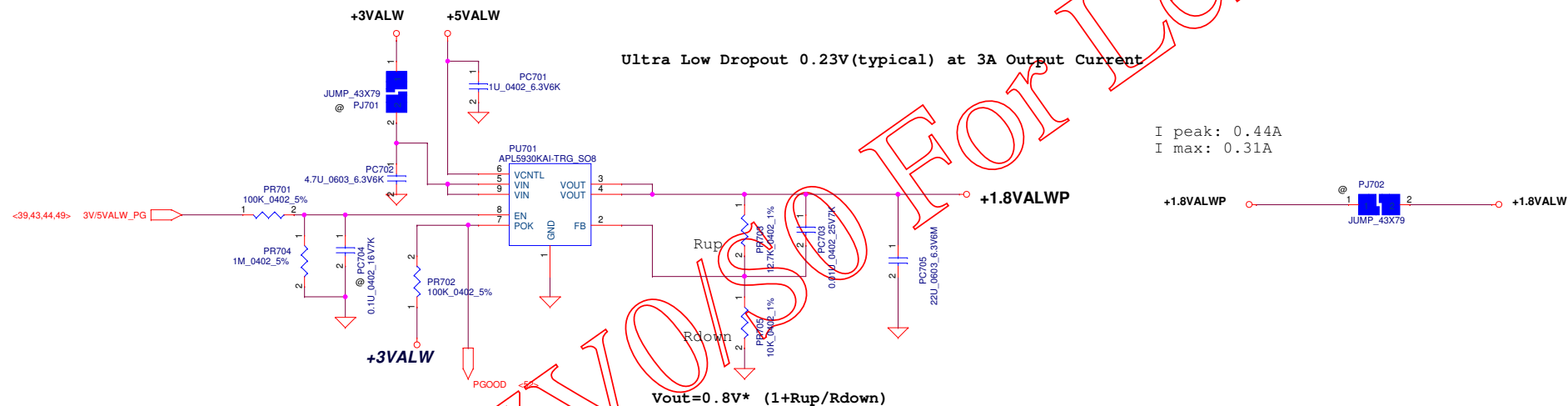
I peak: 0.112A  
I max: 0.08A

Ultra Low Dropout 0.23V(typical) at 3A Output Current

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# Module model information

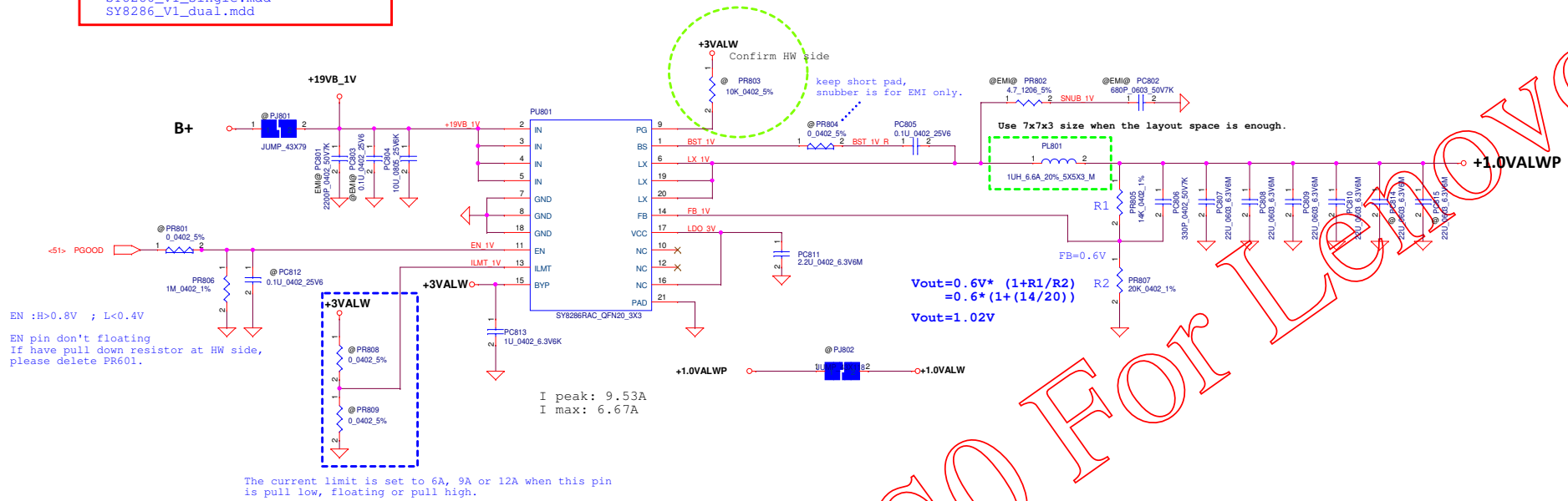
APL5930\_V2.mdd



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# Module model information

SY8286\_V1\_single.mdd  
SY8286\_V1\_dual.mdd



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## CPU CORE

Due to U23e VCC\_GT and GTX merged current spec is TBD in PDDG.  
Please confirm FAE the setting of PRI23, PRI39 PRI63 for U23e GT and GTX merged.

Module model information

NCP81208\_U2223E\_COLAY\_KBL\_V1A.mdd for IC portion

NCP81208\_U2223E\_COLAY\_KBL\_V1B.mdd for SW portion

Copy the schematic to new page,  
the co-lay location maybe changed.

PRI2, PRI8 place near CPU side.  
If the registers are at HW side and POP, PRI2, PRI8 can be canceled

The schematic diagram illustrates the power management block, which is a green-shaded area containing several voltage regulators. The regulators are labeled as follows:

- PR02**: A 100\_0402 1% resistor, connected to **+VCCSA** and **VCCSA\_SENSE**.
- PR03**: A 0\_0402 5% resistor, connected to **VCCSA\_SENSE** and **VSSSA\_SENSE**.
- PR04**: A 0\_0402 5% resistor, connected to **VSSSA\_SENSE** and **VCCCGT**.
- PR05**: A 100\_0402 1% resistor, connected to **VCCCGT** and **VCCCGT\_SENSE**.
- PR06**: A 100\_0402 1% resistor, connected to **VCCCGT\_SENSE** and **VSSCGT\_SENSE**.
- PR07**: A 0\_0402 5% resistor, connected to **VSSCGT\_SENSE** and **VSSCGT\_SENSE**.
- PR08**: A 0\_0402 5% resistor, connected to **VSSCGT\_SENSE** and **VSSCGT\_SENSE**.

The regulators are connected to various power rails and sense lines, including **+VCCSA**, **VCCSA\_SENSE**, **VSSSA\_SENSE**, **+VCCCGT**, **VCCCGT\_SENSE**, **VSSCGT\_SENSE**, and **VSSCGT\_SENSE**. The sense lines are connected to the **SENSE** pins of the regulators.

PRI11, PRI16 place near CPU side.  
If the registers are at HW side and POP, PRI11, PRI16 can be canceled

RPH@IA:  
U42 = 84.5K PRI30,PRI38  
U22 =84.5K PRI30,PRI38(De-pop)

For U22:  
PRI43=De-pop  
For U42:  
PRI43,PRI38=Po

For U22:  
PRI47=1.62K, PRI54=De-pop  
For U42:  
PRI47,PRI54=1.62K

For U22:  
PCI23=De-pop  
For U42:  
PCI23=0.1u

472mV/120uA=3.933K  
Active Point110 degreeC = 4.206K

NCP81218 Operating Frequency  
I/A and GT are 450KHz and SA is 600KHz

RIccMAX2ph:  
For U22:  
PRI63=51.1K  
For U42:  
PRI63=100K  
PRI63 U42@  
100K\_0402\_1%

PSYS:  
Please confirm charger pull low resistance  
Charger side should be unpop.

```

IccMAX@SA= 5A
RlccMAX@SA= 15.8K ---->PRI65

RlccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ---->PRI14

RIOUTSP= 2V/(gm*(Rth+RCCSP)+IccMAX)*DCR
/(RHPSP+Rth+RCCSP)

OCP@SA= 10A
RLIMSP@SA=22.1K ---->PRI5

RLIMSP= 1.4V/(gm*(Rth+RCCSP)*IoutLIMIT*DCR
/(RHPSP+Rth+RCCSP))

Load_line@VA=10.3m
RDREF@SA=1.58K ---->PRI4

RDREFSP= Load_line*(RHPSP+Rth+RCCSP)
(gm + DCR)/(Rth+RCCSP)

```

PRI26 and PRI33 pull high resistor are pop at the end of VR SVID  
Other VR is unpop.

54

PHI3  
100K\_0402\_1%\_B25/50 4250K

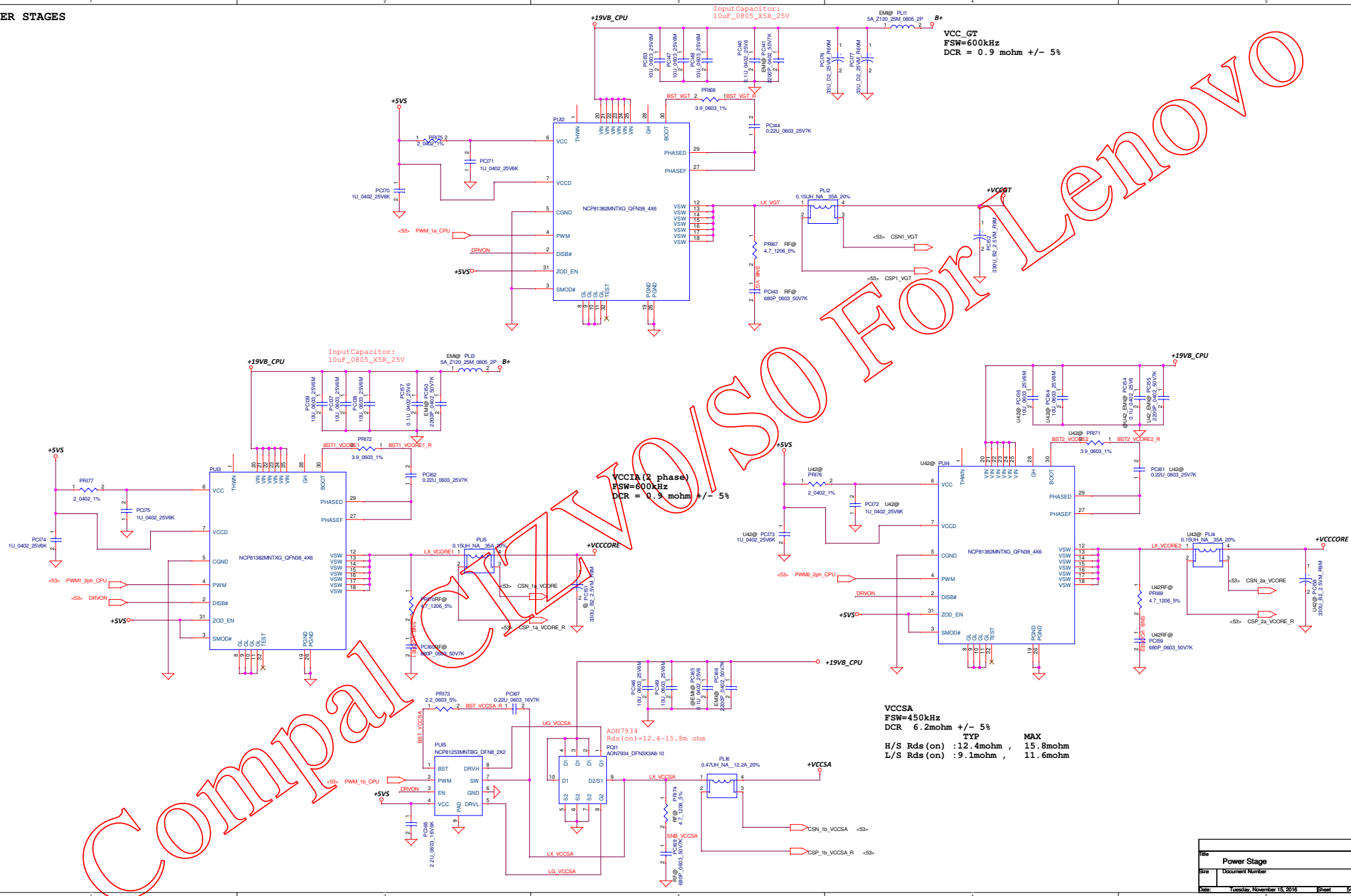
**CORE**

PRI51, PRI58 place near CPU side.  
If the registers are at HW side and POP, PRI51, PRI58 can be canceled

472mV/120uA=3.933K  
Active Point110 degreeC = 4.206K

```
VB00T:
51.1K for debuge setting.
```

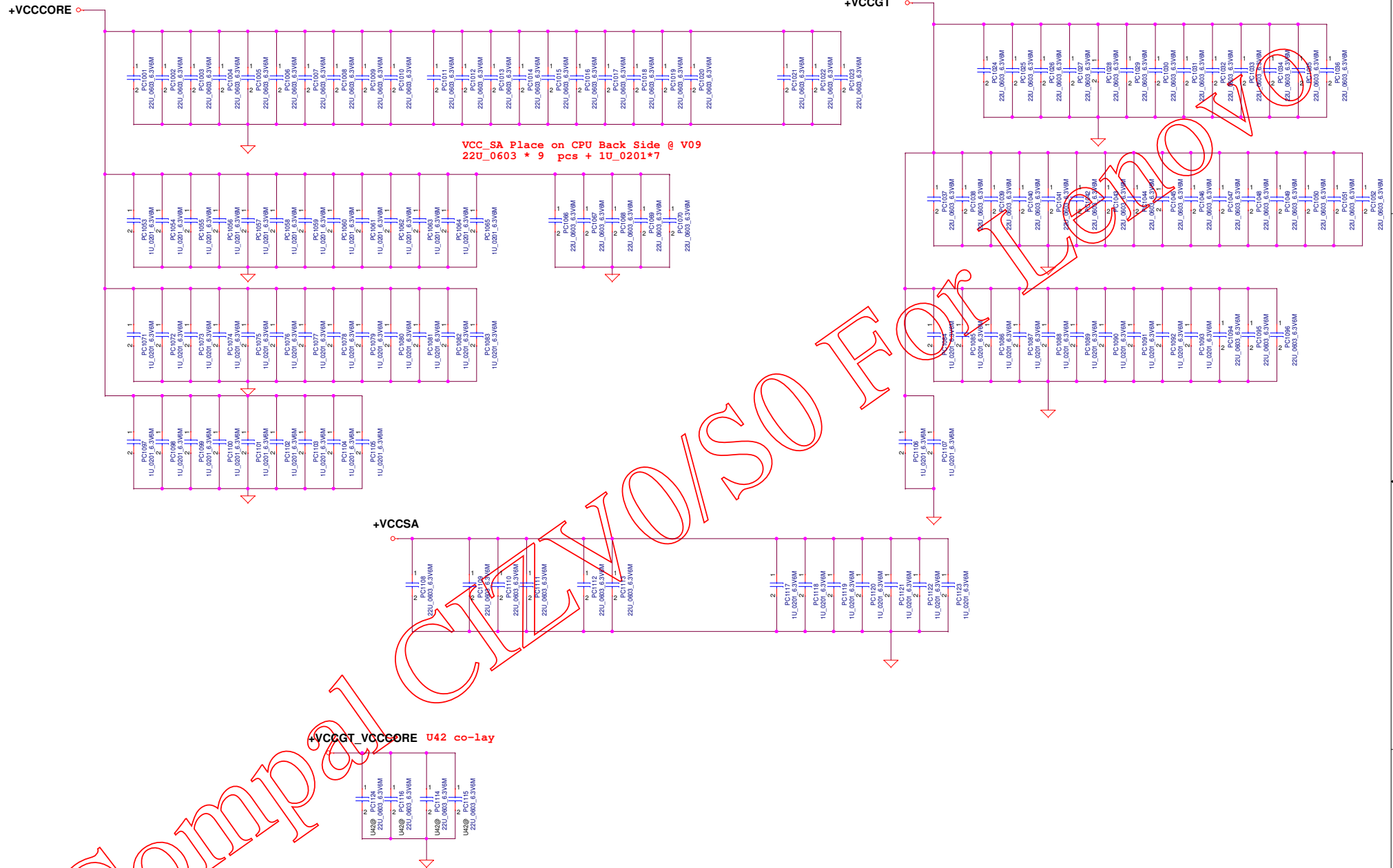
CPU POWER STAGES





VCC\_CORE Place on CPU Back Side @ V09  
22U\_0603 \* 28pcs +1U\_0201\*35 pcs+2.2U\_0402\*3 pcs

VCC\_GT Place on CPU Back Side @ V09  
22U\_0603 \* 32 pcs +1U\_0201\*12 pcs



# 5.OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

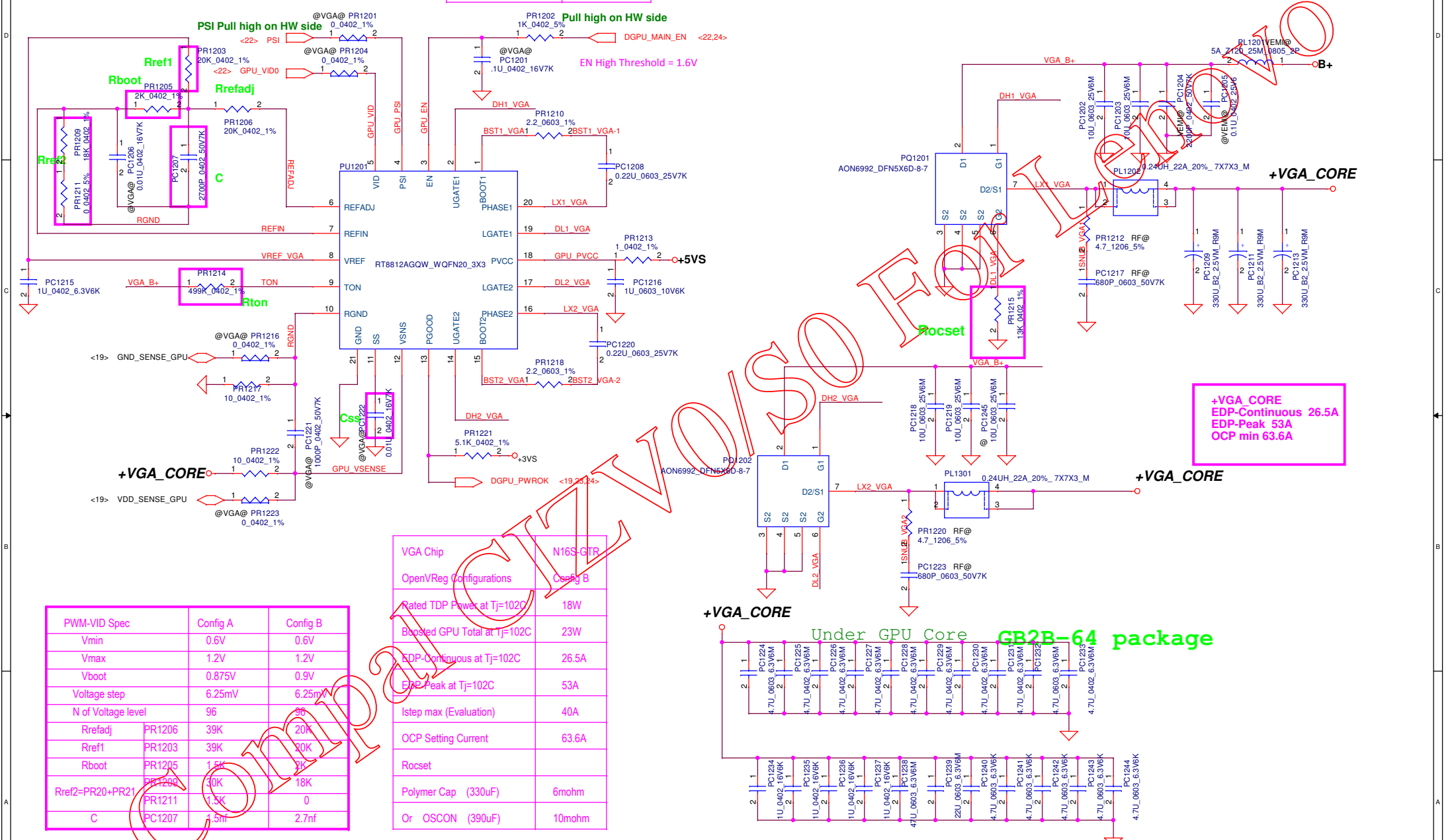
## Dual MOS:AON6992

Q1 Rds(on):  
Typ 6.8 mohm & max 8.6 mohm@Vgs=4.5V

Q2 Rds(on):  
Typ 2.0 mohm & max 2.5 mohm@Vgs=4.5V

## Choke: 0.24uH (Size:7\*7\*3)

Rdc=1.19mohm +5%  
Heat Rating Current=32A  
Saturation Current=22A



PWM-VID Spec	Config A	Config B
Vmin	0.6V	0.6V
Vmax	1.2V	1.2V
Vboot	0.875V	0.9V
Voltage step	6.25mV	6.25mV
N of Voltage level	96	96
Rrefadj	PR1206 39K	20K
Rref1	PR1203 39K	20K
Rboot	PR1205 1.5K	2K
Rref2=PR20+PR21	PR1209 30K	18K
C	PR1211 1.5K	0
	PC1207 1.5nf	2.7nf

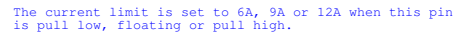
VGA Chip	N16S-GTR
OpenVReg Configurations	Config B
Rated TDP Power at Tj=102C	18W
Boosted GPU Total at Tj=102C	23W
EDP-Continuous at Tj=102C	26.5A
EDP-Peak at Tj=102C	53A
Istep max (Evaluation)	40A
OCP Setting Current	63.6A
Rocset	
Polymer Cap (330uF)	6mohm
Or OSCON (390uF)	10mohm

## +VGA\_CORE

Under GPU Core CB2B-64 package

+VGA\_CORE  
EDP-Continuous 26.5A  
EDP-Peak 53A  
OCP min 63.6A

SY8286\_V1\_single.mdd  
SY8286\_V1\_dual.mdd



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